Appendix B

Design Implementation Description For The Digital Frequency Demodulator

The DFD design implementation is divided into four sections:

1. Analog front end to signal condition and digitize the FM multiplex input.
2. Data channel digital demodulators to provide digital data outputs.
3. Analog reconstruction and conditioning to provide analog outputs.
4. Digital data combiner to provide the parallel data output.

Each of these sections is designed to be completely programmable, in contrast to the analog approach of turning potentiometers, setting switches, or changing plug-in modules.

B.1 Analog Front End

The analog front end section provides identical circuitry for processing two analog FM multiplexes with bandwidths up to 4 MHz. Each multiplex is independently signal conditioned and then digitized to provide a sampled output at 16 MHz. Each demodulator includes a programmable input selector for choosing the desired multiplex. Figure 2 shows the front end processing for one multiplex.

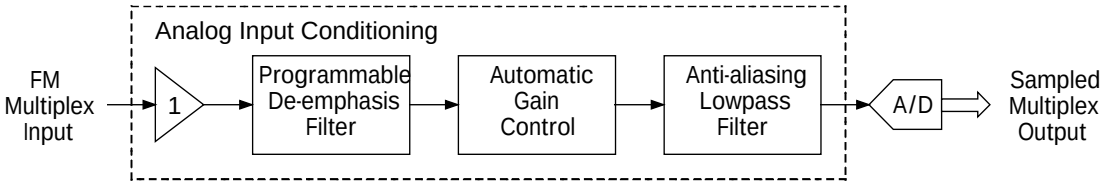


Figure B-1. Analog Front End

An input amplifier buffers the FM multiplex input and feeds it to a user programmable de-emphasis filter, which is programmable from 1 kHz to 1 MHz. This one-pole filter allows the user to shape the amplitude taper of the multiplex input spectrum to correct for the pre-emphasis performed on the FM multiplex prior to recording on tape. The de-emphasized filter output is a multiplex spectrum with uniform amplitude level, which greatly improves the signal-to-noise performance of all channels prior to digitization.

Next, an automatic gain control (AGC) circuit adjusts the overall amplitude of the data to achieve the highest signal resolution prior to digitizing the multiplex. The AGC is designed to provide constant output levels for inputs from 2 mV to 2 V rms.

The anti-aliasing lowpass filter eliminates any frequency terms in the multiplex above 4 MHz. This passive filter provides pre-sample filtering to keep the signal spectrum below the Nyquist rate of the digital data pipeline in the demodulators.

Lastly, the analog input data is digitized using a 12-bit sampling analog-to-digital (A/D) converter at a rate of approximately 16 MHz. By sampling at 4 times the highest input frequency, all multiplex data can be digitized together, thus eliminating the need for programmable anti-aliasing filters. Any remaining unwanted frequencies in the digitized multiplex are digitally filtered out by the digital data demodulator.

B.2 Digital Data Demodulators

Each data channel demodulator contains a digital data demodulator providing a digital output, followed by a reconstruction and conditioning circuit for converting the digital output to an analog output.

The heart of the DFD is the individual digital data demodulator. The FM demodulation process is a series of DSP hardware mathematic algorithm blocks (Figure 3). Because of the extremely high bandwidth of the input data, standard DSP processors (e.g., Texas Instruments TMS320 or Analog Devices 21xx) can not perform the computations fast enough. The DFD uses both Metraplex proprietary ASICs and industry supplied Very Large Scale Integrated (VLSI) modules to implement the DSP functions.

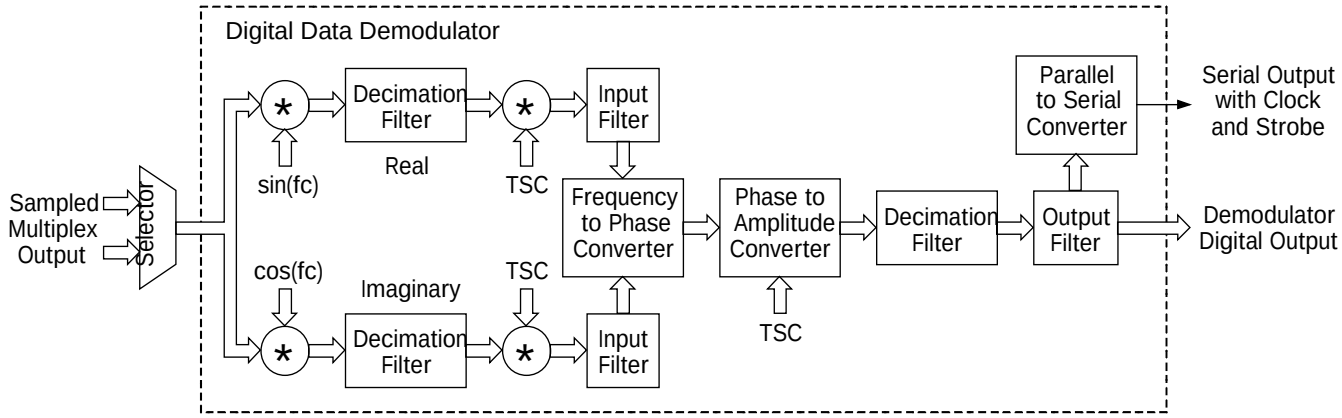


Figure B-2. Digital Data Demodulator

The reason the DFD has such a wide programmable range for each of its data demodulators is the use of independent, ASIC implemented, filter modules for each channel. ASIC gate array technology allows each filter module to be cost effective as well as efficiently packaged. Metraplex developed two new DSP algorithm ASICs for the DFD design, which are joined by previously developed ASICs from the DFM design. Both new ASICs are digital filter modules performing Finite Impulse Response (FIR) algorithms. The first ASIC is a unique decimation filter module and the second ASIC is an oversampling filter module. By creating these fully synchronous DSP filter modules, no circuitry has to be time-shared between channels. This allows the DFD to have essentially perfect time correlation between demodulator channel outputs in the multiplex.

The digital data demodulator design approach in Figure 3 starts with a complex frequency translation of the desired input channel. This translates the desired channel center frequency down to where the demodulated output is centered around DC or 0 Hz. The classical deviation bandpass filter is eliminated because the desired channel can be extracted from the translated multiplex using a digital lowpass filter.

The complex frequency translation is performed using a Metraplex developed ASIC. The ASIC is programmed to the center frequency of the desired channel and generates two waveforms in perfect quadrature (sine and cosine). The digitized FM multiplex is then multiplied by both the real (sine) and imaginary (cosine) portions of the waveform to produce the sum and difference frequency terms of the multiplex with respect to the user programmed center frequency. Since both the real and imaginary data

travel through the ASIC pipelines in parallel, there are an identical number of register delays in each path to maintain perfect time correlation of the two waveforms.

The next stage the demodulator eliminates all unwanted sum and difference frequency terms from the frequency translated multiplex. The first stage of this digital filtering process is the decimation filter, which passes only the data from DC to one-half the Nyquist sample rate. In order to meet the desired wide-band frequency response for each demodulator, a multiple half-band decimation FIR filter was implemented in the Metraplex ASIC. According to the Nyquist sampling theorem, the output of a half-band decimation filter can be resampled at half the original rate without losing any information and causing any aliasing of the input data.

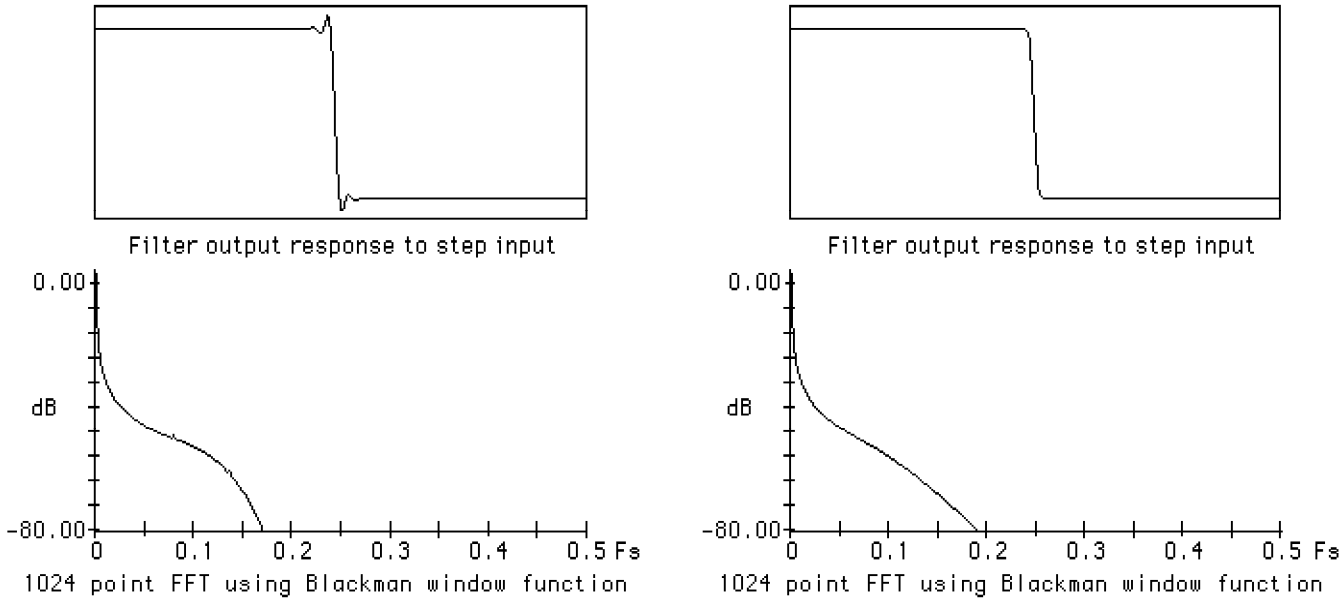
The ASIC decimation filter allows the output decimated data to be fed back into the same half-band filter to be further decimated. This is accomplished by designing the ASIC so that the calculation of the first decimation process takes less than half the decimated sample time. The other half of the available time is used to process a decimation filtering of a higher order. The partial decimation filtered values are stored within the ASIC and controlled by a state machine that determines the appropriate time slot to feedback the partial decimation filter value. The total number of decimations depends on the programmed deviation bandwidth of the channel being demodulated. The decimation filter serves as a preliminary deviation lowpass filter stage, but more importantly, it slows down the digital pipeline clock to allow use of a precision FIR filter as a deviation input filter.

Tape speed compensation (TSC) may be applied to the decimated data prior to the input filter. The output of the TSC demodulator (which is identical to a data demodulator) is used to frequency shift the data demodulator output to compensate for variations in the tape speed during playback of the analog tape recorder. This process is performed using standard VLSI multiplying modules.

Now the real and imaginary pipeline digital data are prepared for the final stage of the deviation input filter. The final stage is another FIR filter with a programmable lowpass cutoff frequency. The DFD microcontroller calculates the filter coefficients using a modified Remez Exchange algorithm from the user entered deviation bandwidth data, and then downloads the filter coefficients to the demodulator hardware. The FIR input filter uses a multiply accumulator VLSI module to perform the digital filtering. The input filter coefficients are optimized to prevent harmonic distortion terms from increasing as the deviation ratio is reduced to one. This is not possible with traditional analog bandpass input filters.

After the input filter, the data passes through a frequency-to-phase converter and then through a phase-to-amplitude converter. The first uses the ratio of the real and imaginary filtered data to convert from the frequency domain to the phase domain by comparing the phase relationship of the quadrature terms. The second converts data from phase domain to the amplitude domain by multiplying the digital data by a scalar value calculated from the user programmed deviation of the channel. Final TSC gain correction is performed on the deviation scalar prior to multiplying the scalar against the phase data.

Finally, the digital pipeline data passes through a digital output filter consisting of another Metraplex decimation filter ASIC and user programmable FIR filter. The decimation filter allows the user to program deviation ratios from 1 to 512. Again, the pipeline data with be decimated to a rate where the output FIR filter can have maximum performance.



a. AC optimized filter response

b. Transient optimized filter response

Figure B-3. Step Response Comparison of Digital FIR Output Filters

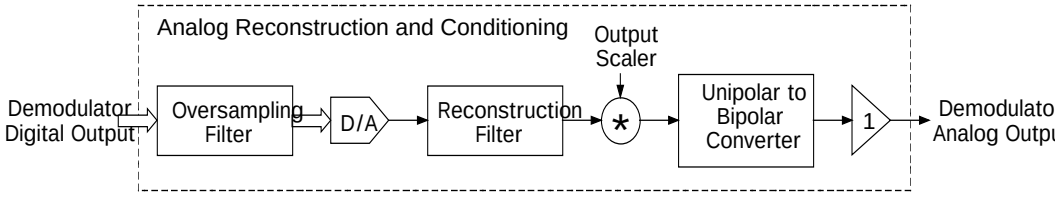
The user has the choice of two different modes of response for the digital output filter (Figure 4). Both modes are FIR constant amplitude, constant delay digital filters. The coefficients for one filter mode are optimized for AC performance and provide a response that is –0.1 dB at cutoff and –60.0 dB at 2.0 times cutoff. This filter mode removes all distortion terms generated in the frequency to amplitude conversion. The coefficients for the other filter mode are optimized for transient or step response performance and provide a response that is –3.0 dB at cutoff and –60 dB at 2.5 to 3.0 times cutoff. This filter mode removes the unwanted overshoot terms on step response input data. The DFD microcontroller calculates the coefficients for the desired output filter mode and downloads them to the demodulator hardware.

B.3 Analog Reconstruction and Conditioning

The analog reconstruction process (Figure 5) must accommodate different sample rates. Digital pipeline output filtered data in each digital demodulator may be running at a different sample rate, depending on the number of decimations needed to achieve the required channel deviation and output filtering. In order to avoid designing switchable analog reconstruction filters, Metraplex developed another proprietary ASIC that performs an oversampling or digital interpolation of the pipeline digital data to speed up the sample rate of the digital data pipeline. This oversampling filter is the reverse of the decimation filter. Instead of feeding back each decimation to reduce the number of output samples, the oversampling filter uses interpolation to increase the number of output samples. To perform the different levels of interpolation, the input data is convolved with the appropriate number of coefficients from the same impulse response. This technique allows the amount of interpolation to be directly related to the number of coefficients stored. The DFD oversamples all digital demodulators to obtain the same output sample rate.

Analog reconstruction is performed using a 12-bit, high speed, digital-to-analog (D/A) converter running at a sample rate that is synchronous to the pipeline system clock. A lowpass reconstruction filter after the D/A removes the digital pipeline clock and associated digital sampling terms caused during the analog reconstruction of the demodulator output. This reconstruction filter has a passband from DC to 500 kHz and covers the entire output frequency bandwidth of each demodulator.

Figure B-4. Analog Reconstruction and Conditioning



Finally, the reconstructed demodulator data is passed through an analog multiplier with scaling factor that allows the user to program the overall maximum output level. A unipolar to bipolar converter provides a summing junction with reference voltage for the user to select unipolar or bipolar analog outputs, as well as positive-going or negative-going unipolar outputs.

B.4 Digital Data Combiner

The digital output of each digital demodulator is available in two forms, parallel by subsystem or serial by individual demodulator. First, each demodulator individually outputs 16-bit serial data, with clock and most significant bit strobe on an output connector on each card. The outputs of all the demodulators in one subsystem may also be combined together using the combiner shown in Figure 1. This combined digital output provides 16-bit parallel data, with 8-bit channel ID, 24-bit time tag, and data clock. The format of the combiner output is set up by the DFD microcontroller and the output format can be displayed on the front panel. The DFD microcontroller calculates the most efficient output format using the different sampling rates for each channel. Individual digital outputs can be easily handled by common computer interfaces available at the data reduction facilities.