

# Appendix A

## Design Implementation Description for the Digital Frequency Oscillator

### A.1 Input Data Front End

The input data front end accepts either analog single ended or differential inputs (figure A-1). The input is received by a differential buffer circuit that can accommodate data bandwidths up to 64 kHz, common mode voltages up to 200 V DC, and voltage inputs up to 10 Vpp. The output of the buffer is connected to an analog switch. The switch is used to isolate the input data signal from the rest of the circuit when performing an internal offset correction to automatically balance the channel.

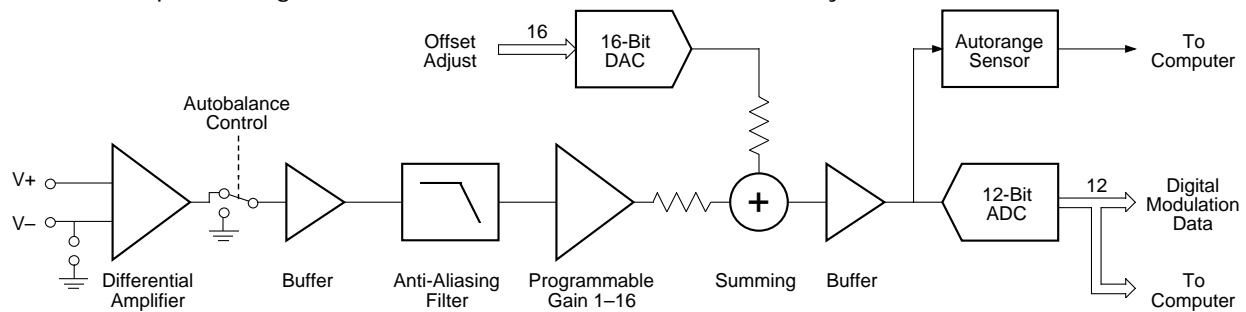


Figure A-1. DFM Channel Front End

The input data signal is then buffered and filtered by a lowpass anti-aliasing filter, which accomplishes two things. First, it filters the data above 64 kHz before sampling. This is necessary because if the data is not band limited prior to sampling, the digital data spectrum will be corrupted by any frequency terms above the Nyquist rate of the sampling system.

Second, the filter corrects for the  $\sin(x)/x$  attenuation effects caused by the sampling process. Most digitizing systems do not attempt to make such corrections. Since the data signal is sampled with pulses of finite width and not with ideal zero-width impulse functions, the resulting signal will be attenuated by a  $\sin(x)/x$  or  $\text{sinc}(x)$  factor, causing the amplitude of the sampled data to decrease as the data frequency increases.<sup>(1)</sup> Therefore, by adding a  $\sin(x)/x$  correction to the anti-aliasing filter, the same fixed frequency anti-aliasing filter and fixed frequency sampling system can be used for all input data frequencies.

After the anti-aliasing filter, the data is passed to a programmable gain amplifier (PGA). This amplifier is computer controlled by user input selection to allow input data voltages from 0.5 Vpp to 8.0 Vpp, in binary gain increments, for  $\pm 100\%$  subcarrier deviations. This corresponds to the gain adjustment potentiometer found in standard analog FM systems.

The output of the PGA is current summed together with a user programmable offset correction that allows the input data to be either unipolar or bipolar, with or without any DC offset. A 16-bit digital to analog converter (DAC) supplies the offset correction, and is also used by the computer to remove any offsets in the analog front end. During an automatic balance sequence, the computer grounds the input to the data channel, by switching the previously discussed analog switch after the input buffer, and reads the sampled data. The offset is measured after sampling and is added to the user selected offset at the DAC.

This internal zeroing eliminates the need to calibrate each subcarrier prior to performing a test. On current analog FM systems, the offset adjustment is performed either by turning a potentiometer or running an automatic calibration sequence. This DAC controlled offset adjustment is also used to perform pre- and post-calibration sequencing of each data channel. Because the computer controls the offset values sent to the offset DAC, the number of steps and the dwell time of each step are user selectable.

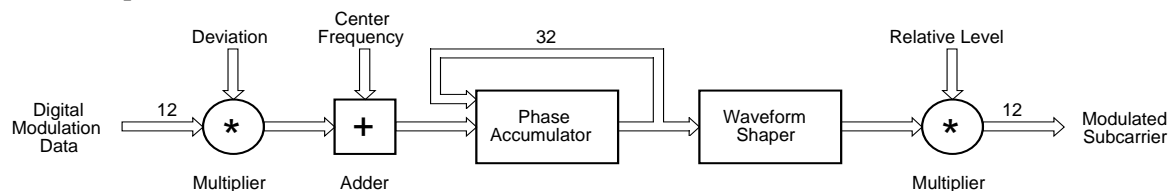
Finally, the input data is digitized using a 12-bit sampling analog to digital converter (ADC). The ADC has a full input range of  $\pm 5$  V DC. By defining that an input voltage range of 8 V<sub>pp</sub> (or 10 V<sub>pp</sub>) corresponds to a  $\pm 100\%$  subcarrier deviation, each data channel can actually be deviated  $\pm 125\%$ , providing a safety margin for overdeviated input signals. The ADC is clocked at approximately 330 kHz, which gives a minimum of 5 points per period for the fastest input frequency of 64 kHz. The ADC clock is derived from the system clock so that all data within the digital pipeline is fully synchronized.

The input to the ADC is also sampled by an automatic ranging circuit. This circuit senses the RMS level of the input data to the ADC and allows the computer to change the gain of the PGA if the full input range of the ADC is not being used.

The digital output of the ADC is the modulation source for the digital modulator. The computer has the ability to read the modulation data and display a representation of the data on the EL panel. This feature provides the user with an indication whether the input data front end is set up correctly to produce the correct amount of subcarrier deviation. Adjustments can be performed by the user to the programmable front end features while the modulation data is being displayed, which gives the user immediate feedback to the changes taken.

## A.2 Digital Modulator

All the hardware algorithms necessary to perform the digital frequency modulation of a subcarrier are built into the ASIC. Figure A-2 illustrates the FM portion of the ASIC. The subcarrier frequency is generated using a numerically controlled oscillator (NCO). The ASIC is programmed with the user selected subcarrier parameters: center frequency, deviation range, and pre-emphasis. After these values are sent to the ASIC, the ASIC performs all subcarrier generation and modulation without computer intervention. The only time the computer communicates to the ASIC is when the user changes a subcarrier parameter.



**Figure A-2 Frequency Modulation Function of the ASIC**

The output of the ADC is registered and fed into the modulation data input of the ASIC. All data inside and outside the modulator is pipeline registered. This means after a function is performed (summing, multiplying, decoding, etc.) the data is clocked into a register that maintains synchronization of the digital pipeline. All data channels have the same number of pipeline delays, so all data from channel to channel will be perfectly time correlated.

The digital input modulation data is scaled by a digital multiplier with a computer calculated value from the user selected deviation range of the subcarrier. The ASIC is designed to allow deviation scaling from 0.5% to 50.0% of the selected center frequency of a subcarrier. Therefore, as different deviation values are chosen, the deviation multiplier scales the ADC data to allow 12-bit resolution (4096 unique steps).

Model Number	Maximum Number of Channels per Mux			
	Mux 1	Mux 2	Mux 3	Mux 4
DFM-36 (36 channels)	8	8	8	8
	12	12	12	0
	16	20	0	0
	8	8	20	0
	12	24	0	0
DFM-32 (32 channels)	32	0	0	0
	8	8	8	8
	12	12	8	0
	16	16	0	0
	8	8	16	0
DFM-28 (28 channels)	12	20	0	0
	12	0	0	0
	8	8	8	4
	12	12	4	0
	16	12	0	0
DFM-24 (24 channels)	8	8	12	0
	12	16	0	0
	28	0	0	0
	8	8	8	0
	12	12	0	0
DFM-20 (20 channels)	16	8	0	0
	24	0	0	0
	8	8	4	0
	12	8	0	0
DFM-16 (16 channels)	16	4	0	0
	8	0	0	0
	12	0	0	0
(12 channels)	8	4	0	0
(8 channels)	12	0	0	0
(4 channels)	8	0	0	0
	4	0	0	0

**Figure A-3. Multiplex Configurations for DFM Models**

After the modulation data is scaled for deviation, the data is summed with a user selected center frequency value. The user can select any subcarrier frequency from 256 Hz to 4,194,304 Hz. The computer calculates the appropriate value to obtain the desired subcarrier center frequency.

The output of the center frequency summer is fed into a phase accumulator, which is the heart of the NCO. The input data to the accumulator represents the phase step for each clock cycle, and the output of the phase accumulator at any time corresponds to the phase of the programmed frequency. The accumulator overflows between 359 and 0 degrees, and the rate at which the accumulator overflows is

equal to the output rate of the subcarrier. The phase accumulator inside the ASIC is 32 bits wide and is synchronized to the system clock which is running at  $2^{24}$  Hz. The frequency resolution of the phase accumulator is equal to the clock frequency divided by the number of bits in the accumulator, yielding  $2^{-8}$  or 3.9 millihertz.

The output of the phase accumulator, which represents the phase of the waveform being synthesized, is converted to a sine wave in the wave shaping function. This function calculates the true value for the sine wave at the phase angle that is being entered. By calculating the true value of the sine wave and having a crystal controlled phase accumulator with excellent phase resolution, there are essentially no harmonic distortion terms generated in the sine wave, as there are in present analog wideband FM recording systems. The output from the waveform shaper is a 12-bit full scale digital sine wave value that is then scaled against a user entered relative output level, or pre-emphasis value. Pre-emphasis scaling is done using a 12-bit, two's complement multiplier. Entering 0 dB for the pre-emphasis value leaves the digital sine wave at full scale. The user can program the pre-emphasis value of each subcarrier from 0 dB to -20 dB.

### **A.3 Digital Summing**

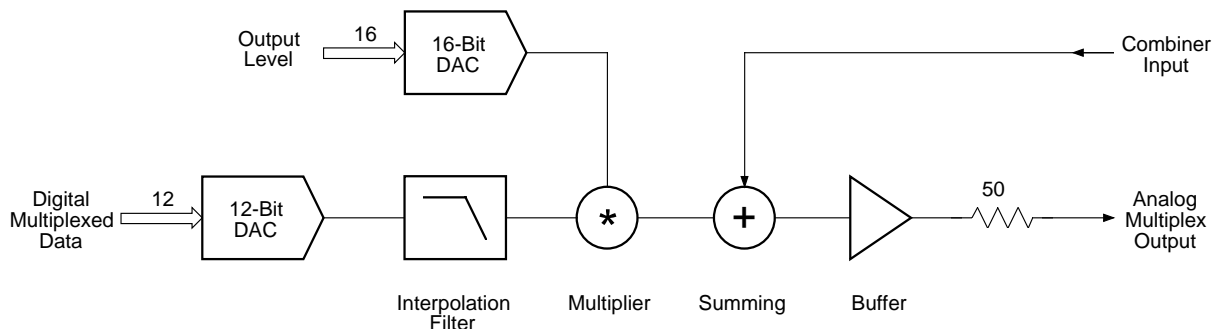
The digital summing function multiplexes together the user selected subcarriers. As previously stated, each DFM subsystem can have up to 36 data channels plus 2 channels in a common multiplex. These channels can be configured for output in up to 4 different multiplexes. Table 15-1 illustrates the different configurations, listing the number of channels for each output multiplex.

Four data channel front ends and digital modulators are placed on one printed circuit board, the Quad Digital Modulator card. The four modulator outputs are digitally summed together prior to exiting the board by a second proprietary ASIC. This approach greatly reduces the number of connection lines within the DFM subsystem, so that only 12 data lines are required for each group of four channels.

Each Quad Digital Modulator card sends the initial summed data to the Summing card. The Summing card is designed to direct the different digital subcarriers to the appropriate summing points in order to achieve the desired multiplex configuration. The second ASIC, also used on the Summing card, was designed to have the flexibility to program different pipeline delays in the summing system in order to maintain time correlation between all subcarriers in all the different multiplex configurations. Each multiplex has a selection control register that is computer programmed to turn on or off the common multiplex and to direct the multiplexed subcarriers to the appropriate multiplex outputs.

### **A.4 Analog Reconstruction**

Analog reconstruction of the digitally multiplexed subcarriers is accomplished on the Quad Output card using a high speed 12-bit DAC (figure 15-4). The DAC has a settling time twice as fast as the rate that data is processed in the pipeline. The DAC must also be able to output a bipolar sine wave without inducing distortion terms into the multiplexed subcarriers. During the digital to analog conversion, the system clock frequency is modulated with the frequency of the digitally synthesized subcarrier. The digital system clock frequency term is removed from the multiplex using a lowpass interpolation filter. This filter has a passband from DC to 4 MHz and provides excellent attenuation at the digital pipeline rate of  $2^{24}$  or approximately 16 MHz. The interpolation filter also provides a constant group delay through the passband of the filter in order not to cause time correlation errors within the multiplexed subcarrier data.



**Figure A-4. Analog Reconstruction**

Each filtered, reconstructed multiplex output is passed to a bipolar analog multiplier. The user can program the output level of each multiplex to the appropriate level for the tape recorder system that the data will be stored on. A 16-bit DAC programmed by the computer is used to generate the scale factor to multiply the multiplexed subcarriers. This programmable multiplex output level is similar to adjusting the output potentiometer on present analog FM recording data systems.

Each output scaled multiplex is available from the DFM subsystem as a 50-ohm driven output on a BNC connector. A summing amplifier also permits an external signal to be combined with the multiplex.

### **A.5 Controlling Computer**

The DFM contains an IBM PC compatible, single board Computer card to simplify data processing and file exchange with remote systems. A Metraplex installed ROM on the card contains the boot program for initializing the system when power is turned on. The Computer card is mounted on an ISA Buffer card, which drives the motherboard bus.

The DFM Master Subsystem includes a 3.5-inch disk drive for storing the DFM Master Software program and format files.

During operation, the computer in the Master Subsystem checks for the presence of other subsystems, reads the subsystem number and card configuration, and initializes the subsystems by downloading format configuration parameters.

Communications between subsystems are handled by GPIB interface cards that plug into the motherboard of each subsystem. Subsystems are daisy-chained together using standard GPIB cables. An IBM PC/AT compatible computer with 760410-3 GPIB card may be added to the interface as a Computer Subsystem.

A Host Computer can control several DFM Systems. This requires that a second GPIB card be installed in the DFM Master Subsystem. The second GPIB interface turns the entire DFM System into a single subsystem of a larger GPIB network.

Remote control operation is also possible using the Computer card's RS-232 port. The DFM software will accept simple commands from a remote terminal.