MULITPLEXER / DEMULTIPLEXER

USING A

CCSDS FORMAT

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I. DESIGN BACKGROUND

ORIGINAL: DATA COLLECTOR SYSTEM

Digitize Multiple AGC signals

Add IRIG & NASA Time Code

Add Voice channel

Keep output BW low for linear tape recorders

NEXT REQUIREMENT:
DIGITAL DATA MUX/DEMUX

Accept PCM streams up to 20 Mbps

Optionally include all of above

- Digital input stream (2 units cascaded)

- Option modules for MDM

CONSISTANT DESIGN GOALS:

Keep cost down

Simplicity of operation

Accept wide variety of inputs

- High Speed Synchronous Data (PCM)
- Low Speed Asynchronous Data (commands...)
- Time Code
- Audio
- Analogs (slow speed AGCs thru high speed premod signals)
- Specials

Accept wide variety of links

- Direct connects
- Tape Recorders
- Communications links
- Networks

Ability to scale composite bit rate

II. CCSDS PACKETIZED TELEMETRY OFFERS :

LAYERED ARCHITECTURE

WELL DEFINED I/O PER FUNCTION

APPLICATION DATA FORMAT
is DECOUPLED from
COMPOSITE FORMAT

ABILITY TO CHANGE THE ENDS WITHOUT
REDISGNING THE MIDDLE

BUFFERED SERVICE (vs QUEUED)

RECONSTRUCTION OF INPUT DATA :
USER'S CHOICE :

DIRECT CPU INGEST, S/W PROCESSING

RECONSTRUCT FOR INGEST VIA
LEGACY EQUIP.

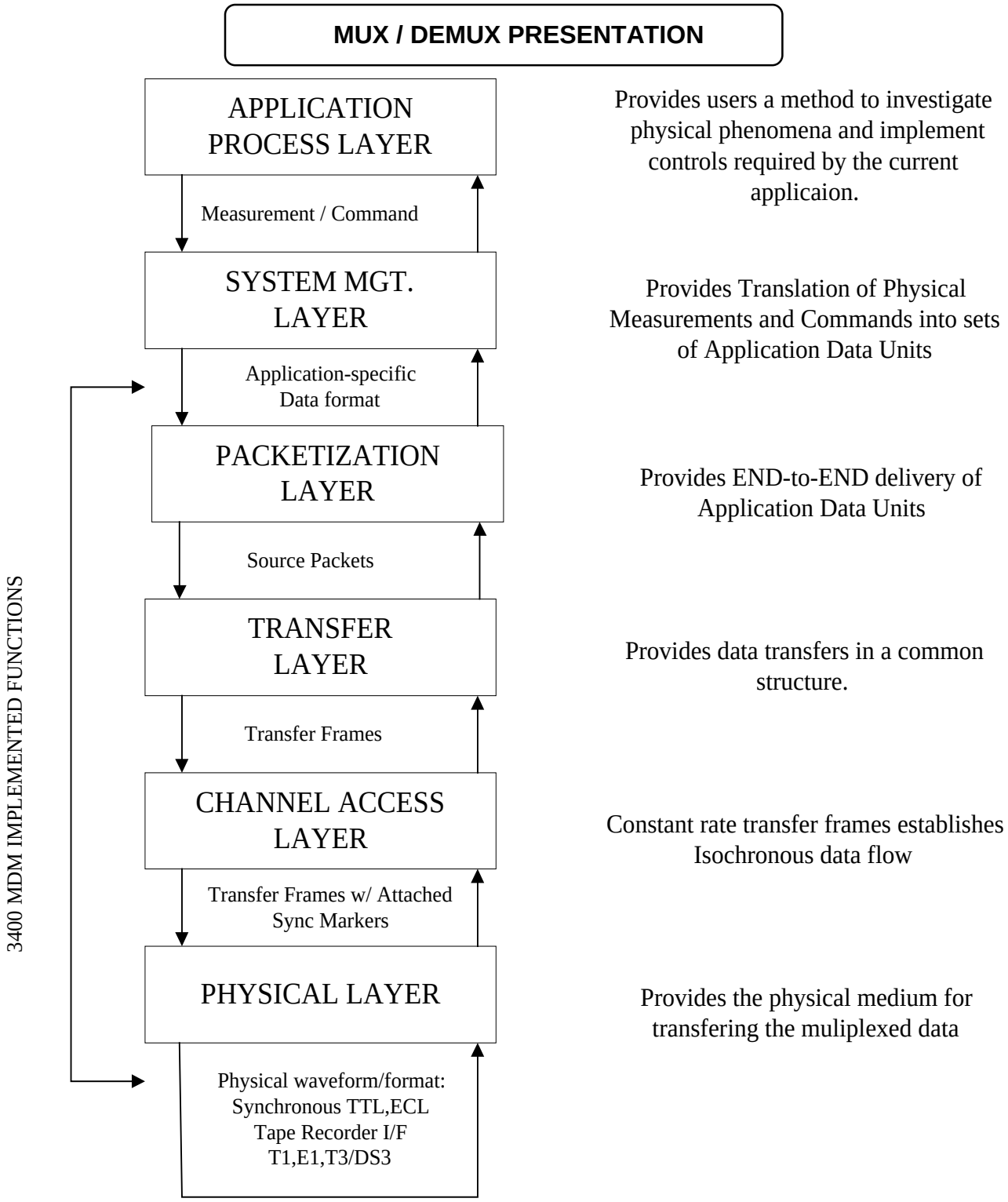


Figure 1-1 LAYERED SERVICE MODEL

SOURCE PACKET PRIMARY HEADER

VERSION NUMBER	PACKET IDENTIFICATION			PACKET SEQUENCE CONTROL		PACKET DATA LENGTH
	TYPE INDICATOR	PACKET 2ND HEADER FLAG	APPLICATION PROCESS IDENTIFIER	GROUPING FLAGS	SOURCE SEQUENCE COUNT	
3 Bits	1 Bit	1 Bit	11 Bits 2 Bits	14 Bits	16 Bits	

---------- 2 Bytes ---------- ---------- 2 Bytes ---------- ---------- 2 Bytes ------

TRANSFER FRAME PRIMARY HEADER

TRANS-FER FRAME VERSION #	TRANSFER FRAME IDENTIFICATION			MASTER CHANNEL FRAME COUNT	VIRTUAL CHANNEL FRAME COUNT	TRANSFER FRAME DATA FIELD STATUS				
	SPACE-CRAFT ID	VIRTUAL CHANNEL ID	OPER. CONTROL FIELD FLAG			TRANS. FRAME 2ND HDR FLAG	SYNCH. FLAG	PACKET ORDER FLAG	SEGMENT LENGTH ID	FIRST HEADER POINTER
2 Bits	10 Bits	3 Bits	1 Bit	8 Bits	8 Bits	1 Bit	1 Bit	1 Bit	2 Bits	11 Bits

----------2 Octets---------- ---- 2 Octets ---- ---------- 2 Octets ----------

SHADED AREAS MARK FIXED FIELDS

III. APPLYING CCSDS TO A MUX/DEMUX UNIT

UNIT BLOCK DIAGRAM APPROXIMATES
PACKETIZED TELEMETRY FUNCTIONAL DIAGRAM

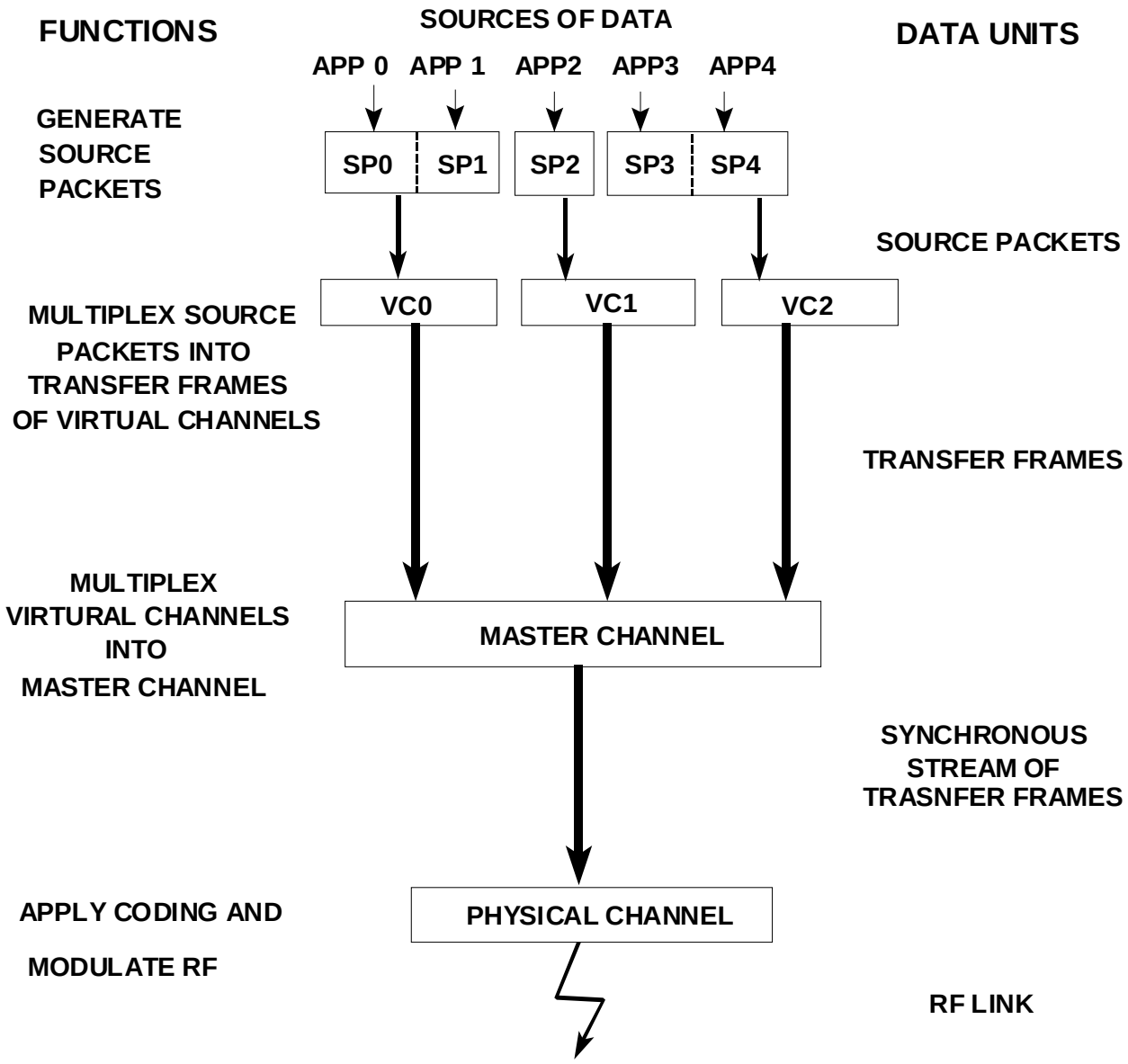
SAMPLING TO IMPLEMENT BUFFERED SERVICE

FPGAs :
HARDWARE vs FIRMWARE
DEDICATED LOGIC vs PROCESSORS

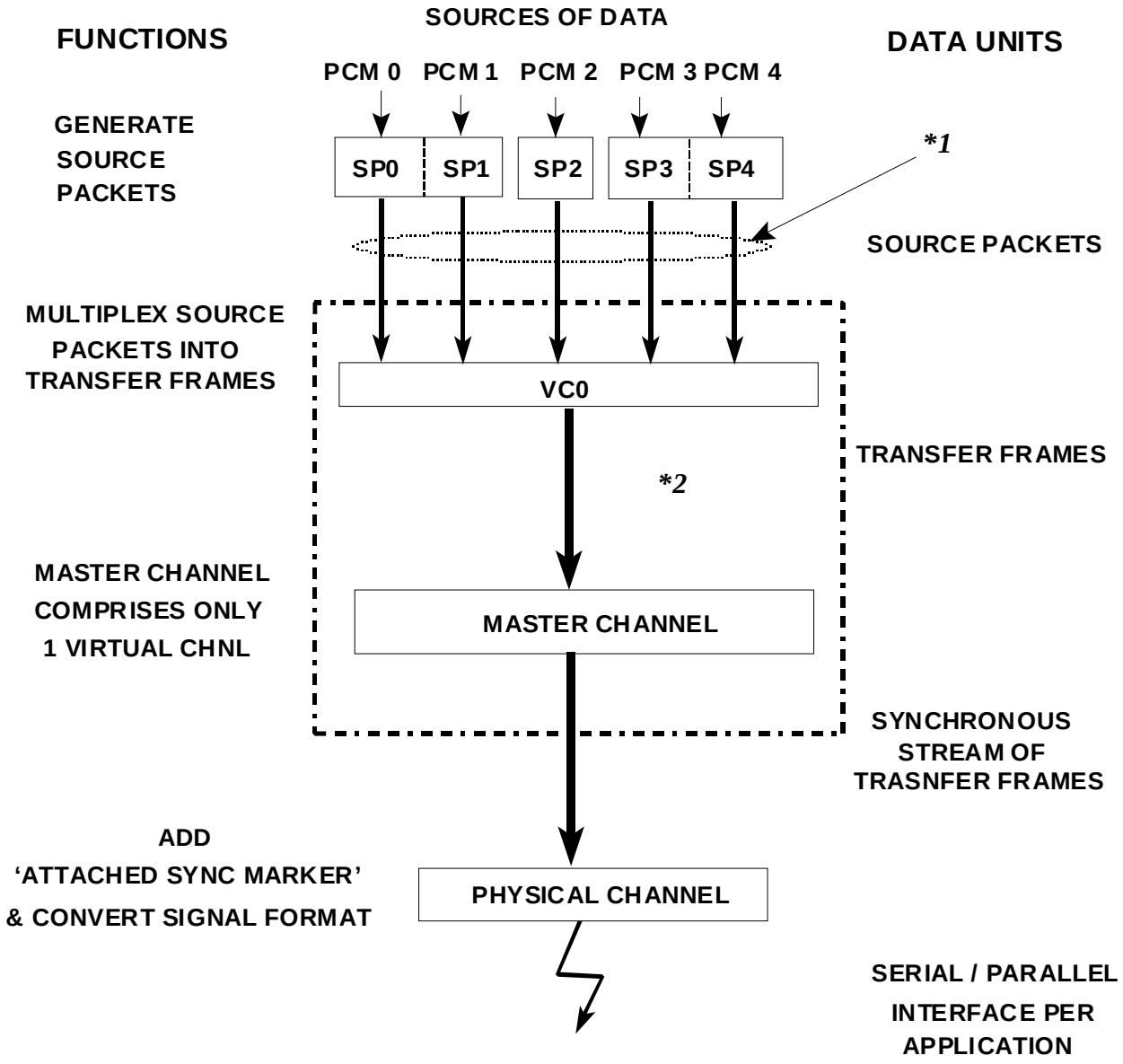
LINK DESIGNS

SERIAL & PARALLEL I/F 'PHYSICAL LAYER'

MUX / DEMUX PRESENTATION



MUX / DEMUX PRESENTATION



IV. RESULTS

UNIT CHANNEL I/O INCLUDES

- PCM TELEMETRY
- LOW RATE COMMAND AND ASYNC DATA
- VOICE
- TIME CODE
- ADCs & DACs to come
- T1 to come

UNITS SUPPORT

- HELICAL SCAN TAPE RECORDERS
- DIRECT LINKS
- SATELITE MODEMS
- T3/DS3

EASE OF OPERATION

- PCM ONLY : COMPOSITE RATE SELECTION
- NO FORMAT DESCRIPTIONS
- AUTO. BIT RATE TRACKING
- DATA ACTIVITY MAY CHANGE DURING SESSION

OVERHEAD CALCULATION, MODEL 3432

EACH ‘SAMPLE INTERVAL’ (SI) =

8 TRANSFER FRAMES @ 1024 BYTES/FRAME
pr 65536 BITS TOTAL

8 TRANFER FRAME OVERHEAD BITS ARE:
8 * 96 = 768 BITS

16 SOURCE PACKET OVERHEAD BITS ARE:
16 * 48 = 768 BITS

65536 BITS - 1536 OVERHEAD BITS = 64000 DATA BITS

OR, 1536 / 64000 = 2.4% OVERHEAD

THROUGHPUT DELAY :

SI/BIT RATE

EX: 2.048 MILLISECONDS @ 32 Mbps

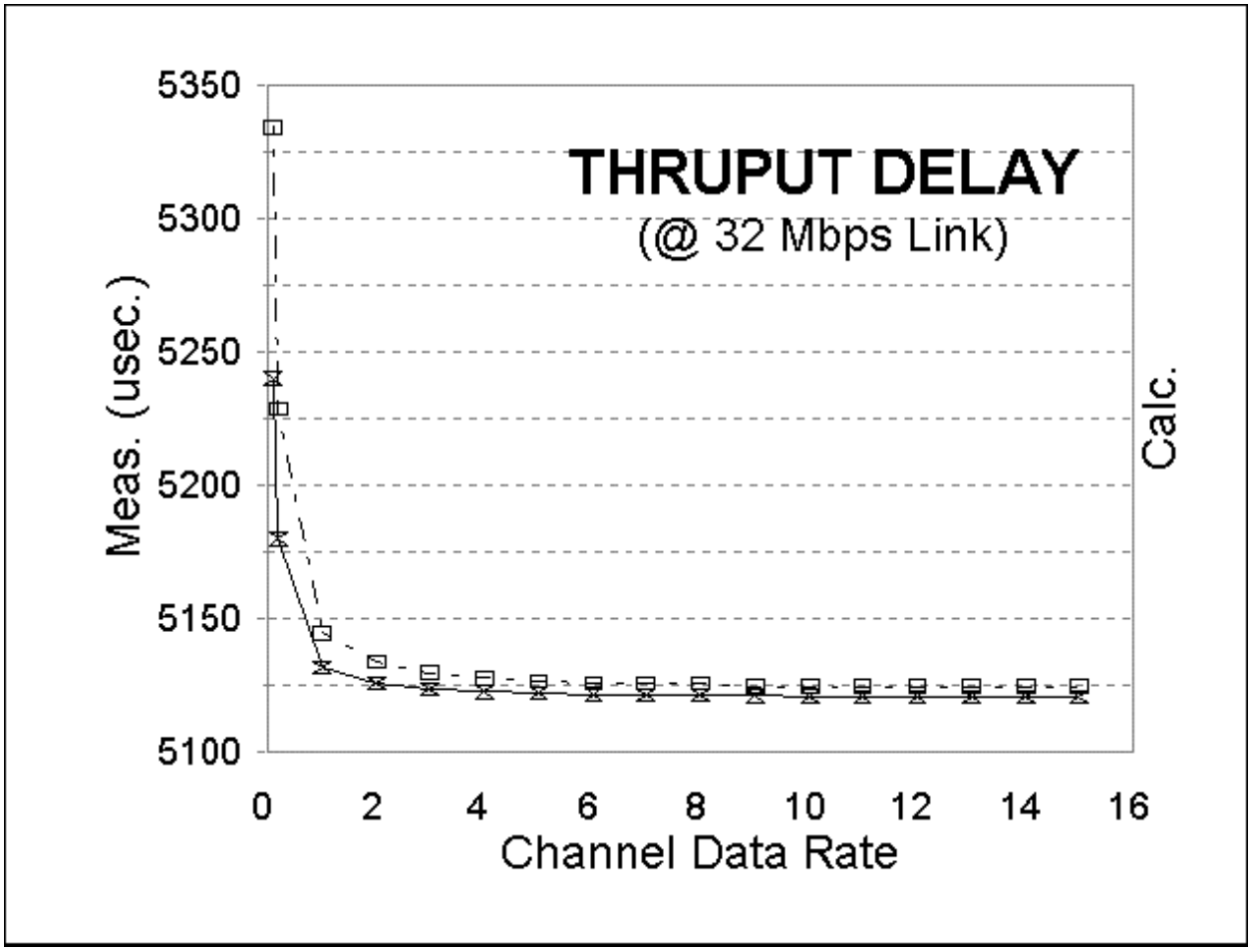
CHANNEL - CHANNEL SKEW :

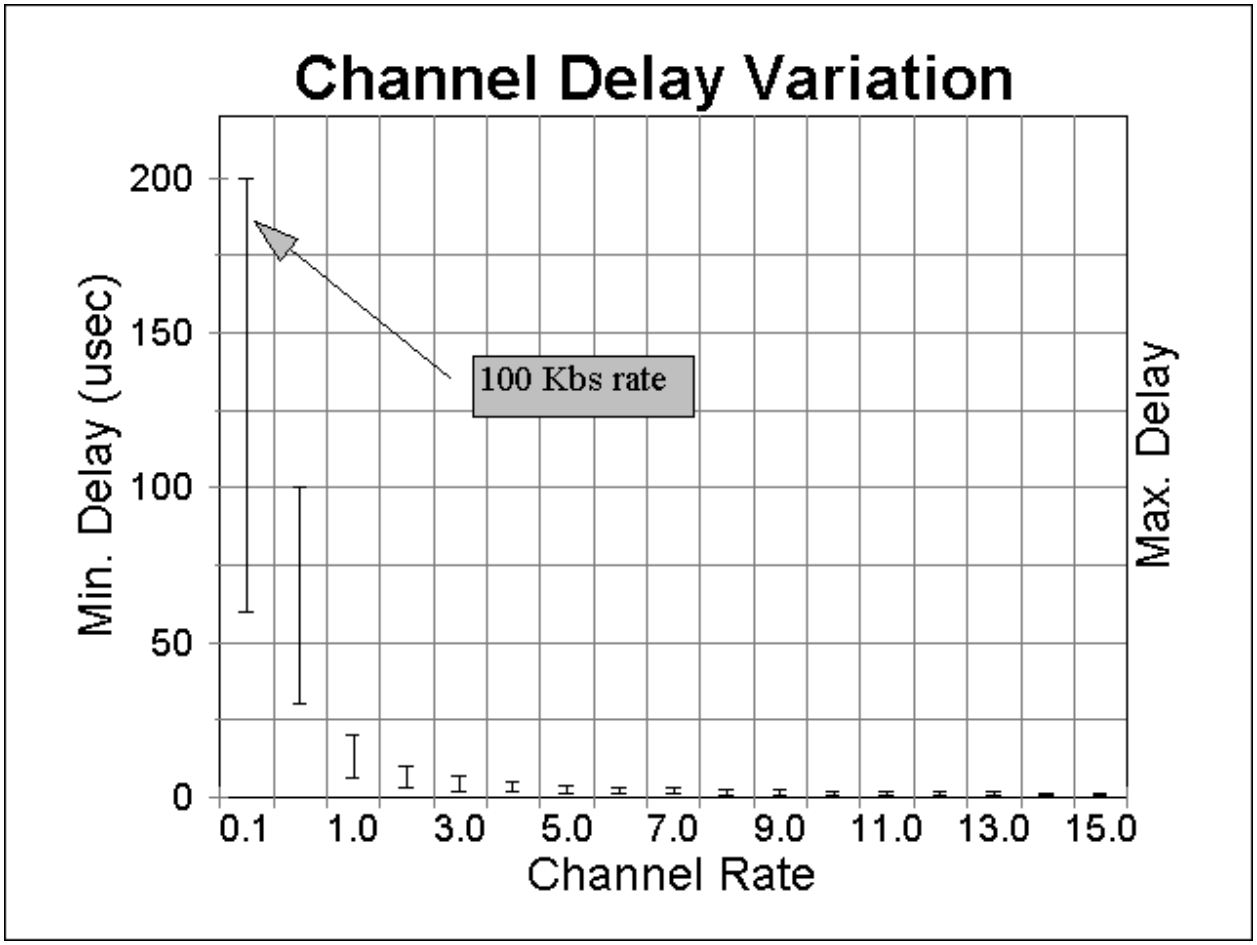
SOURCE PACKET GENERATOR DEPENDENT

HIGH RATE (LOW $$) : 20 BITS
LOW RATE : <10 MICROSECONDS

OUTPUT RECONSTRUCTED CLOCK JITTER:

< 1% TYPICAL


THRUPUT DELAY
(@ 32 Mbps Link)
Meas. (usec.)
Calc.
5350
5300
5250
5200
5150
5100
0
2
4
6
8
10
12
14
16
Channel Data Rate


Channel Delay Variation
Min. Delay (usec)
200
150
100
50
0
100 Kbs rate
Max. Delay
0.1
1.0
3.0
5.0
7.0
9.0
11.0
13.0
15.0
Channel Rate


CLOCK-TO-CLOCK JITTER
(32 Mbs Link)
Meas'd (Jitter/Freq.)
Calc'd
0.04
0.03
0.02
0.01
0
0
2
4
6
8
10
Channel Rate

SUMMARY : DESIGN GOALS MET

LOW COST UNIT

VERY EASY TO OPERATE

FLEXIBLE INPUT CHANNELS

FLEXIBLE COMPOSITE OUTPUT FORMAT