

Magnetic RAM

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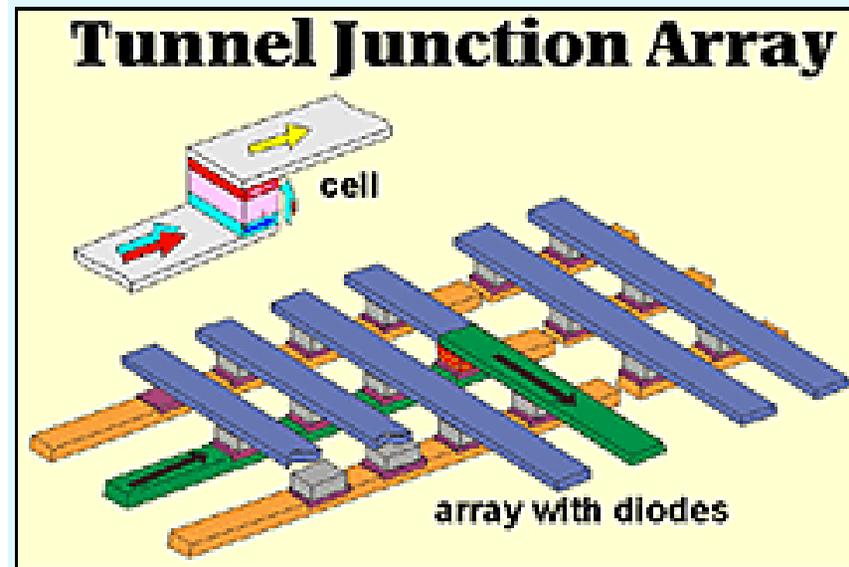
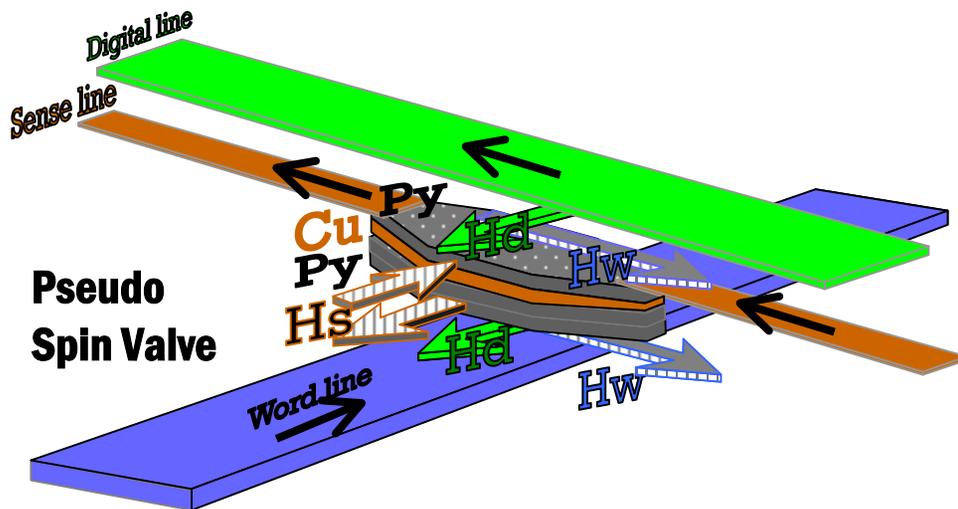
The logo for THIC Inc. features the text "THIC Inc." in a bold, black, sans-serif font. The "THIC" part is set against a light brown, textured rectangular background, while "Inc." is on a white background. A thick, dark brown horizontal bar is positioned below the text.

Magnetic (Magnetoresistive) RAM is it coming and what is it?

A resistance of a conductor, insulator or semiconductor depends on whether two magnets adjacent to it are magnetized in the same or opposite directions.

- The magnets do not forget.
- Non-volatile memory with non-destructive readout.
- Turn on the computer or cell phone and the memory is there.

MRAM



Few in the semiconducting industry want MRAM,
but they are slightly worried about being caught unawares.
If it is coming, they want to control it.

**A serious commitment to MRAM would be \$100,000,000 over 5 years.
A group of us thought we had that funding in March 2000,
but that evaporated along with some other things, like the NASDAC.**

In 1999 Stu Wolf (DARPA) and Gary Prinz (NRL) went to Japan
to see what was going on in MRAM.

They discovered almost nothing.

But their visit woke up the Japanese semiconductor industry
and now there is activity in Japan in MRAM.

There are two geometries for MRAM, current in plane and current perpendicular to the plane. In either case the resistance is read using two sets of perpendicular lines.

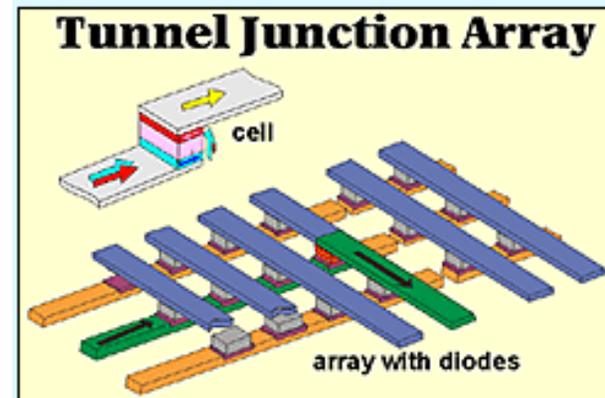
For current in plane, a change in resistance is measured along a line which senses whether a given element increases or decreases its resistance when a bit is addressed. This requires one transistor per line.

For current perpendicular to the plane, the resistance is compared directly to a reference. This requires one diode per bit.

For current perpendicular to the plane, the sandwiched resistor can be either a tunnel junction or a conductor.

The money is on the tunnel junction at this time.

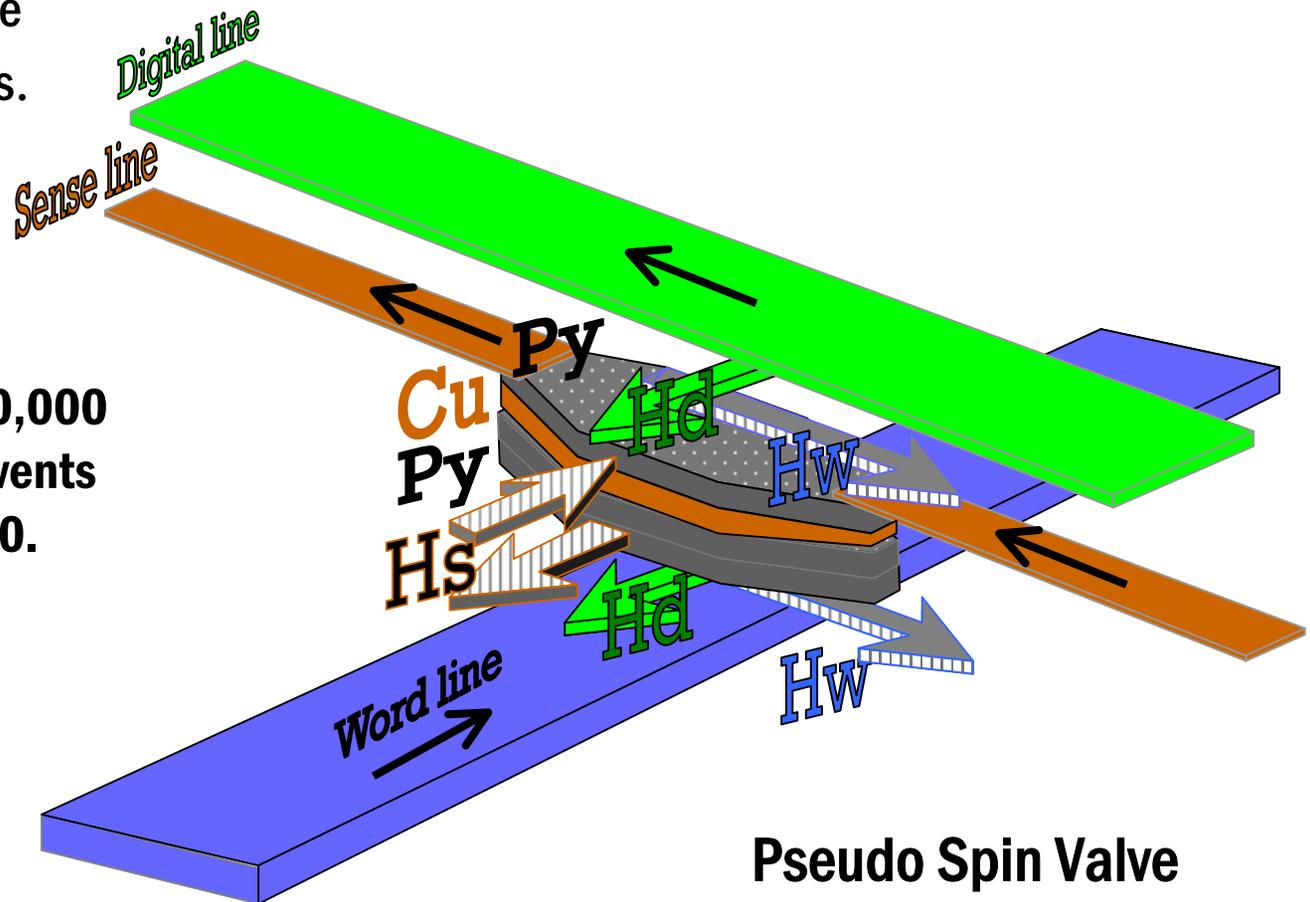
In any case, circuitry is not the basic problem. There are fantastic new tools out there for looking at circuits on the picosecond time scale.



Over a period of three years at Motorola and Honeywell, I measured the resistance changes on the switching of magnetic elements for a variety of designs using psuedo spin valves.

Over a period of five years, now at the Center for Interactive Micromagnetics at Virginia State University, I have used modern micromagnetic theory to calculate what should happen to the resistance when a magnet switches.

I have measured $\sim 100,000$ individual switching events and calculated $\sim 5,000$.



To me, at least, the problem is erratic behavior.

On a given wafer a bit design appears at least once on each die.

The variation in the switching of that design from die to die when the bits all switch by the same mode, is less than the variation of a single bit that switches by more than one mode from time to time;

the mode change can be triggered by a thermal fluctuation

One must control the selection of the mode of switching.

When the bits are large, > 400 nm in width, the problem is that there are several modes of switching for one bit.

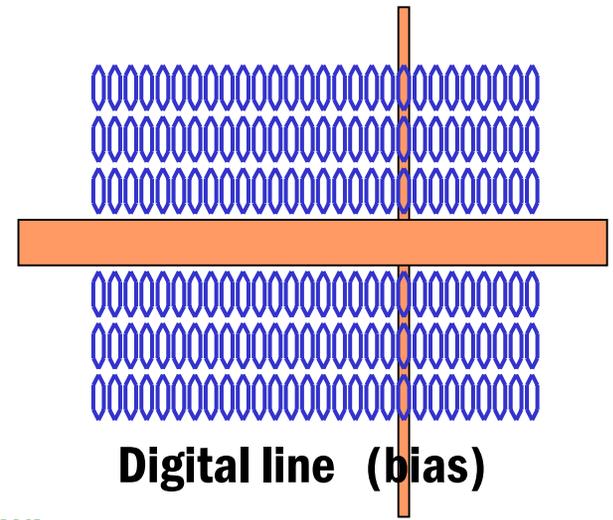
When the bits are small, < 100 nm in width, the problem is that the switching modes are different from one bit to the next.

This is the selectivity problem that I want to address here.

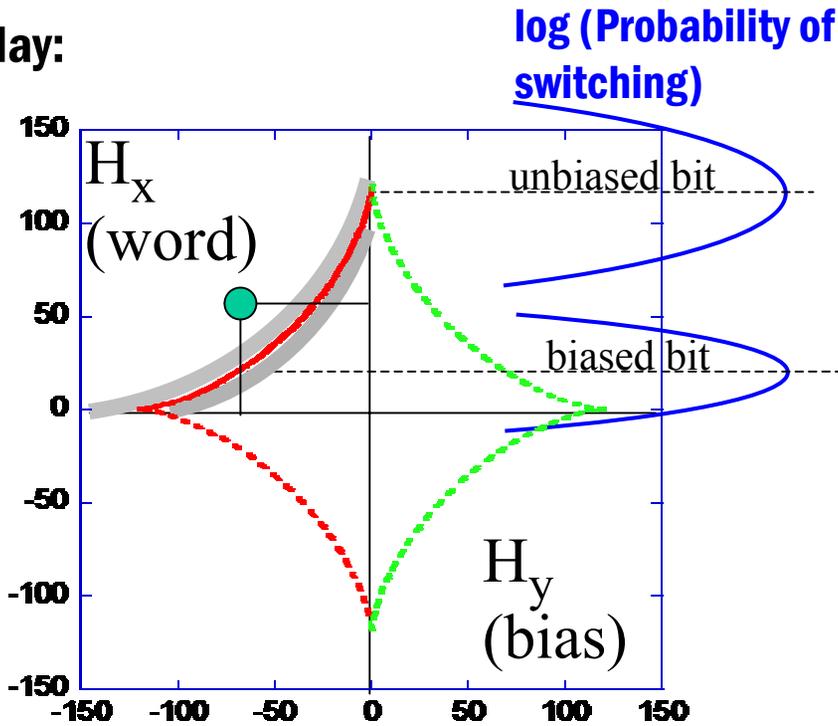
Selection

Neither the Word line nor the Digital line should change the bit, only the combination; regardless of the variations from bit to bit.

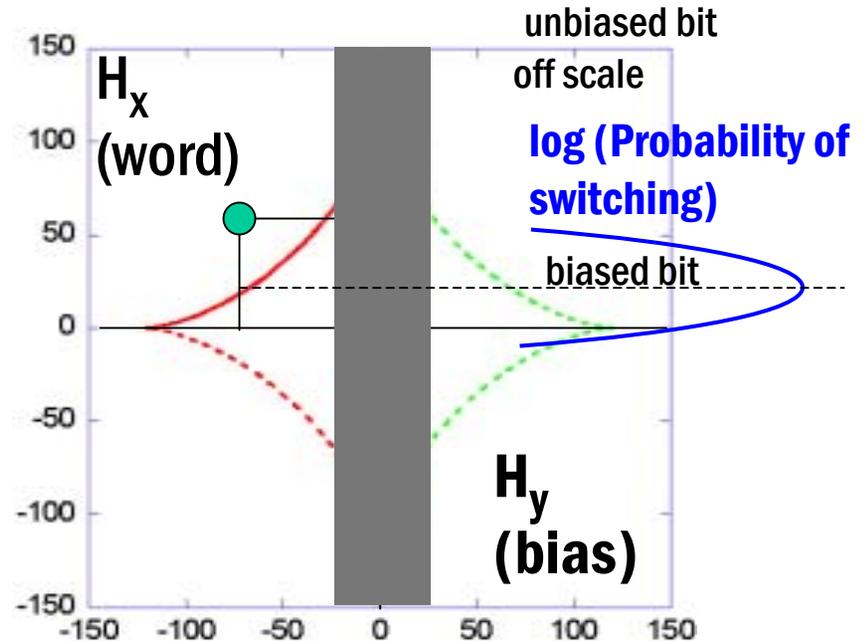
Word line
(switching)



today:



tomorrow:



The ideal is to make every bit go by the same mode if biased and never to go if not biased.

MRAM patterned bits have sizes dictated by compatibility with Silicon technology. MRAM is back-end technology. All of the circuitry is in the silicon wafer except for the magnetic elements and some conducting lines attached to the silicon wafer via via's.

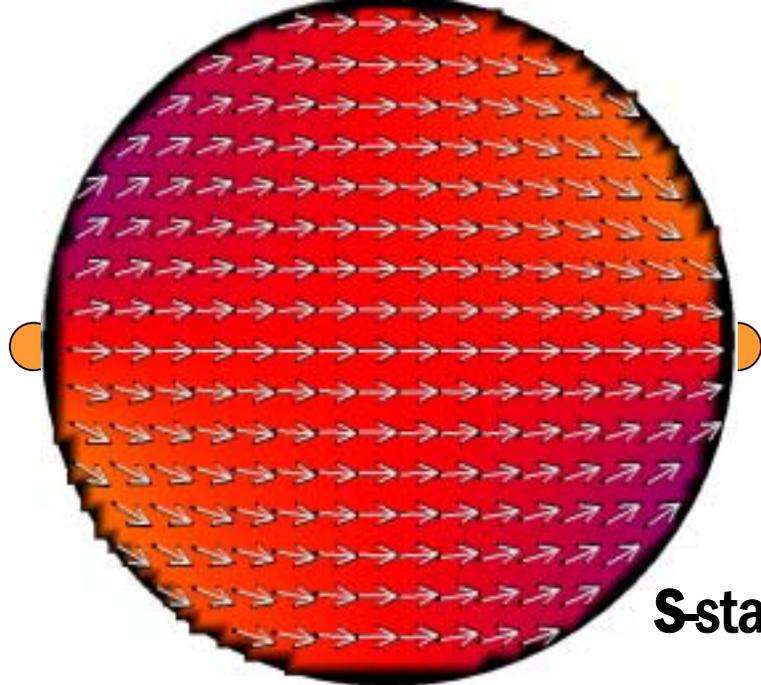
Silicon technology is at 100 nm and the sights are set at still smaller dimensions. Most of the current work is on larger magnetic bits.

Theoretically the magnetic performance would improve with decreasing size. The magnetoresistance effects depend mostly on the thickness of the films. No loss of sensitivity is expected from decreasing both the length and width of a pattern element.

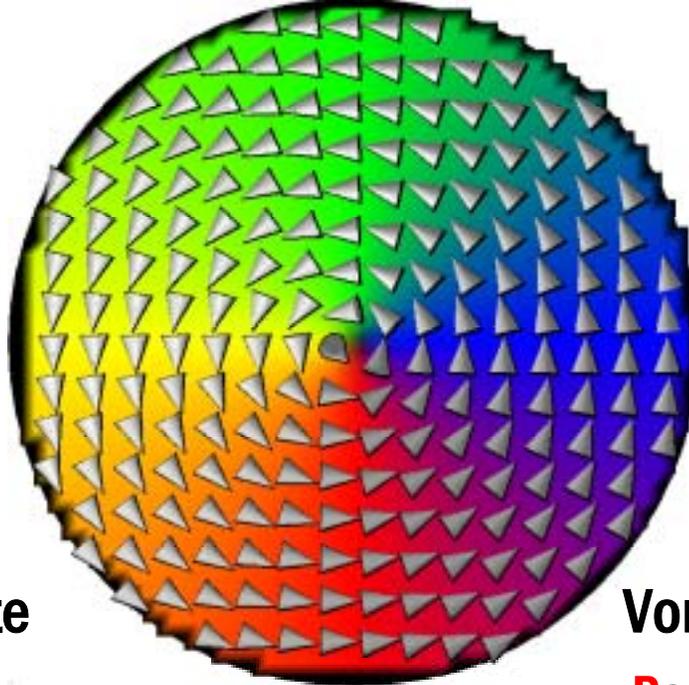
If one works at the edge of patterning technology, shape is not well defined. One can talk about pixels per bit. The ultimate memory is one pixel per bit, but that can only work if one has intrinsic anisotropy.

Current designs use shape to obtain anisotropy and that calls for at least two pixels per bit. I will talk about designs that use at least two pixels.

96 nm disc



S-state



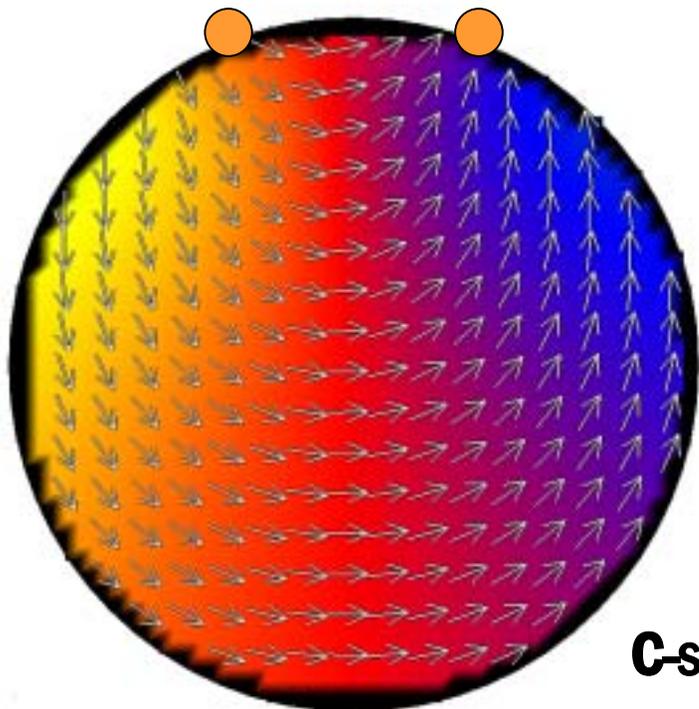
Vortex

One pixel states.

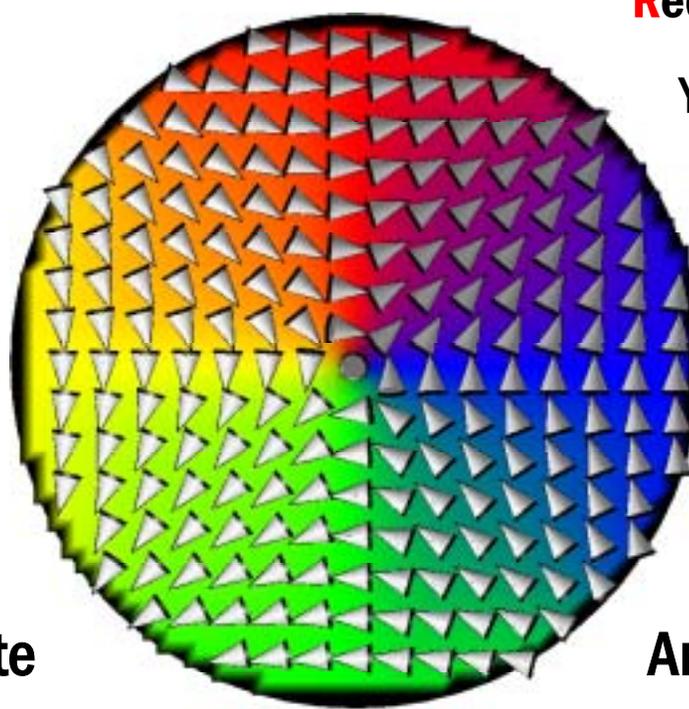
Red is to the right

Yellow is down

Blue is up



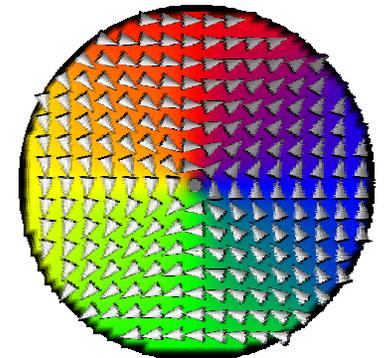
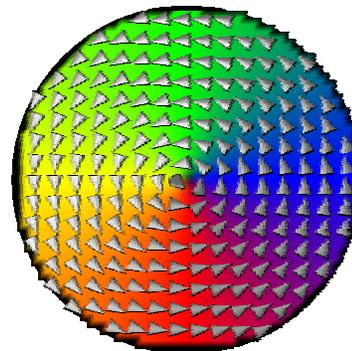
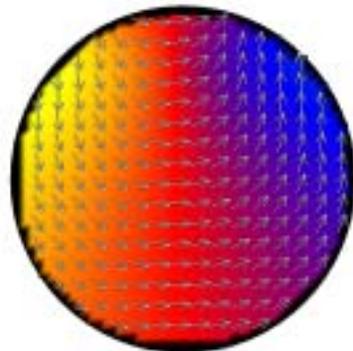
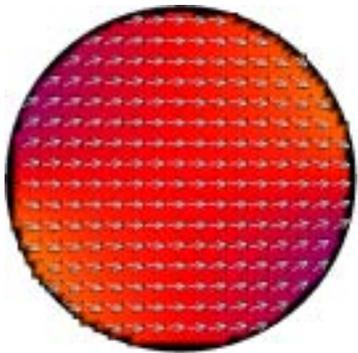
C-state



Anti-vortex

Comparison of energies for different configurations in a 4 nm thick circle of radius 48 nm with the magnetization of Fe, but without anisotropy, no applied fields.

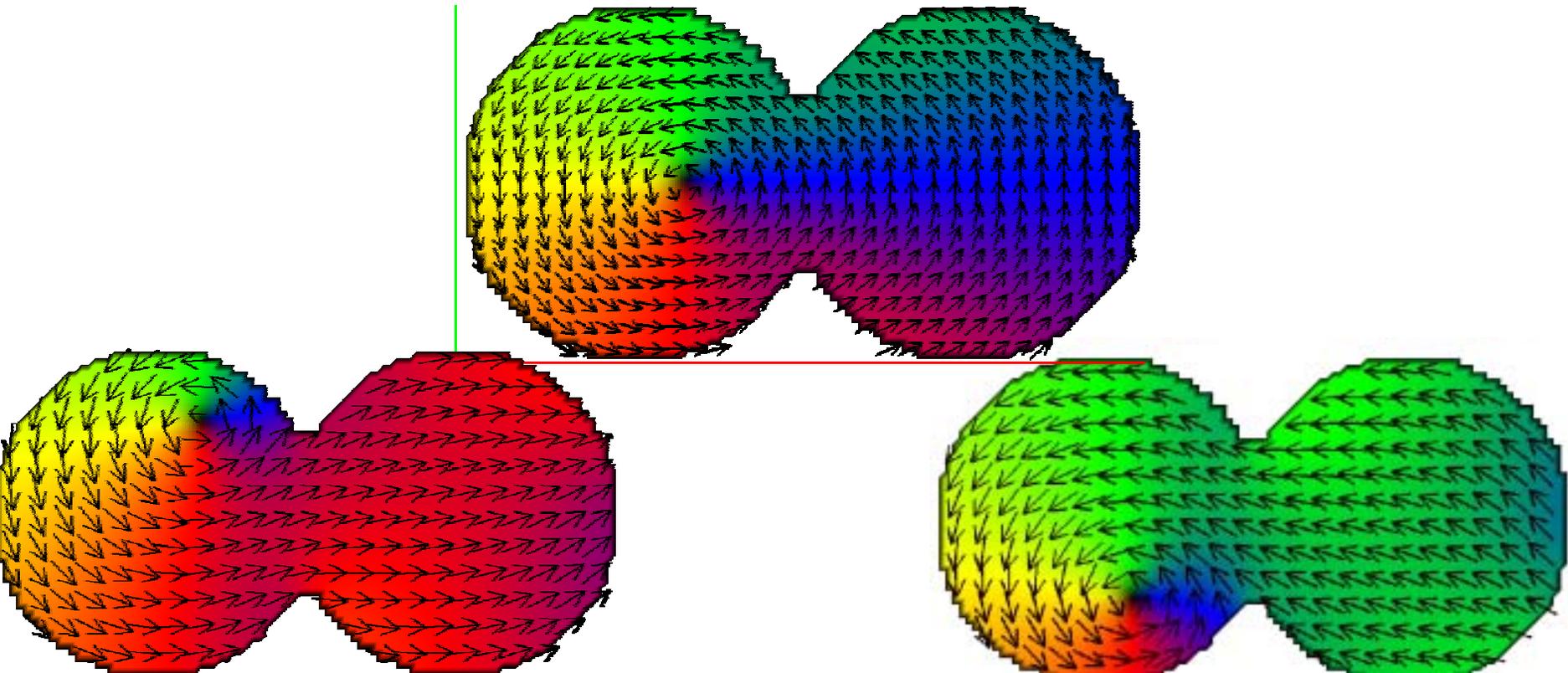
Configuration	M		Energies in picoergs		
	M	direction	magnetostatic	exchange	total
uniform (100)	1.00000	(1,0,0)	28.5420	0.0000	28.5420
uniform (110)	1.00000	(1,1,0)	28.5423	0.0000	28.5423
S-state (100)	0.97043	(1,0,0)	23.8911	1.0525	24.9436
S-state (110)	0.96986	(1,1,0)	23.7486	1.0446	24.7933
C-state	0.67685	(0,1,0)	20.1462	4.0467	24.1930
vortex	0.00582	(0,0,1)	1.4189	10.2897	11.7086
anti-vortex	0.00702	(0,0,1)	38.7789	10.8994	49.6783

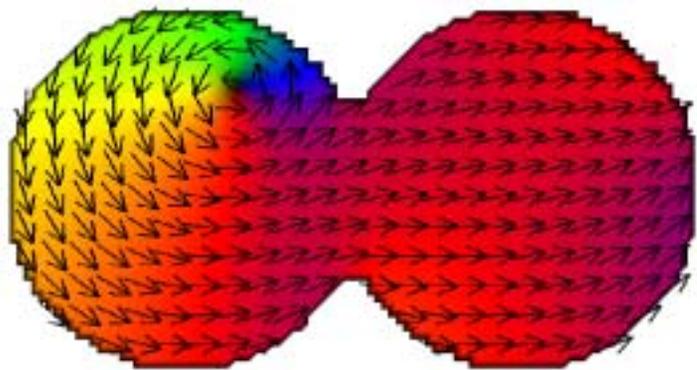


Magnetic Random Access Memories, Brown's Paradox and Hysterons

Anthony S. Arrott, Virginia State University, Petersburg, VA

A novel design for magnetic random access memory elements, called hysterons, is presented. It uses the interaction between two regions of magnetization. In one the process of reversal is almost uniform rotation of a magnetically hard system. In the other it is the reversible motion of a vortex that makes it a magnetically soft system. The magnetostatic interaction between the two regions is anisotropic and hysteretic. The magnetic softness permits using thicker elements that are more stable against temperature fluctuations while having low switching fields.

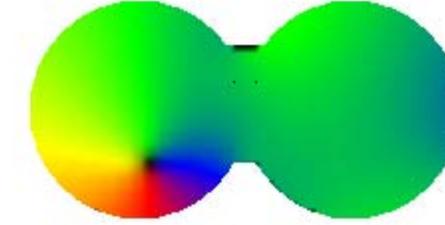
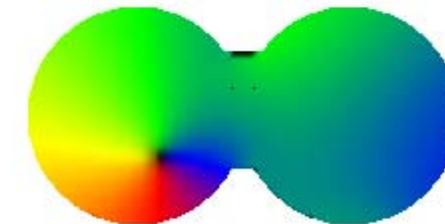
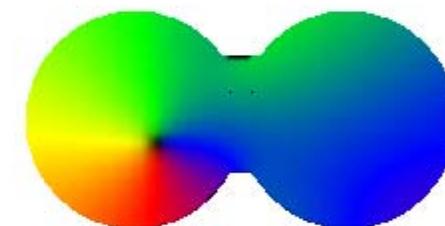
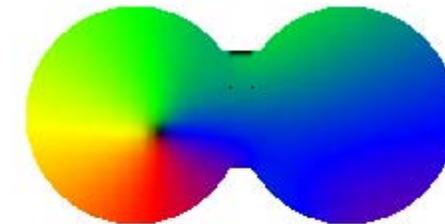
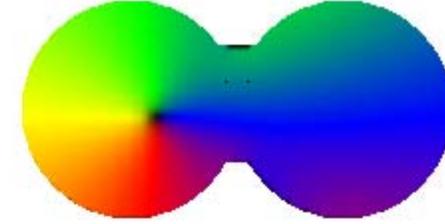
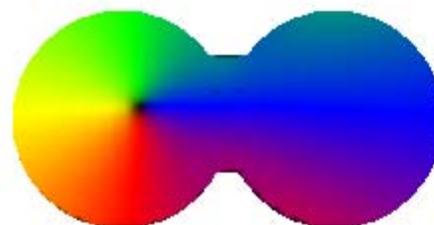
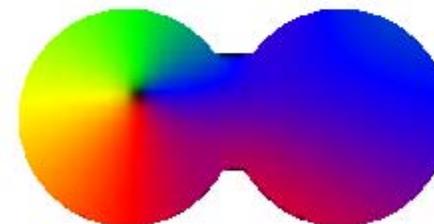
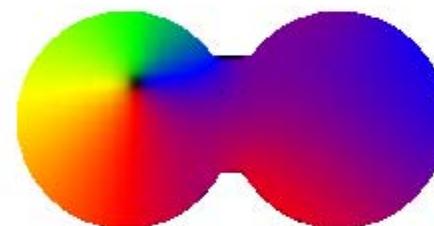
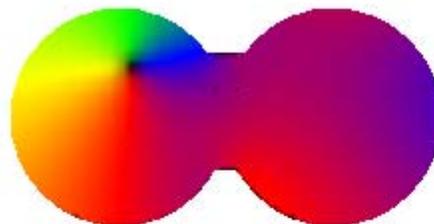
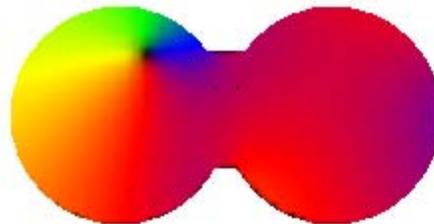
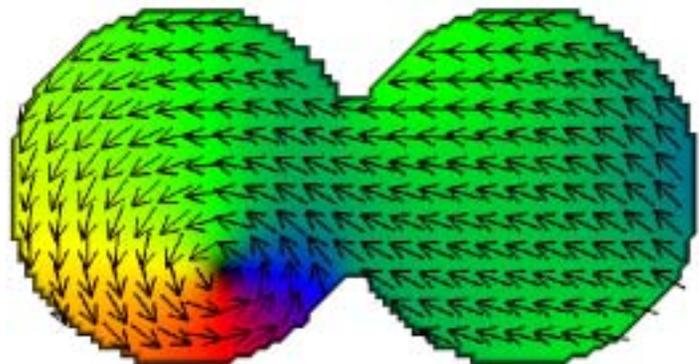




200 x 100 x 8 nm³ hysteron



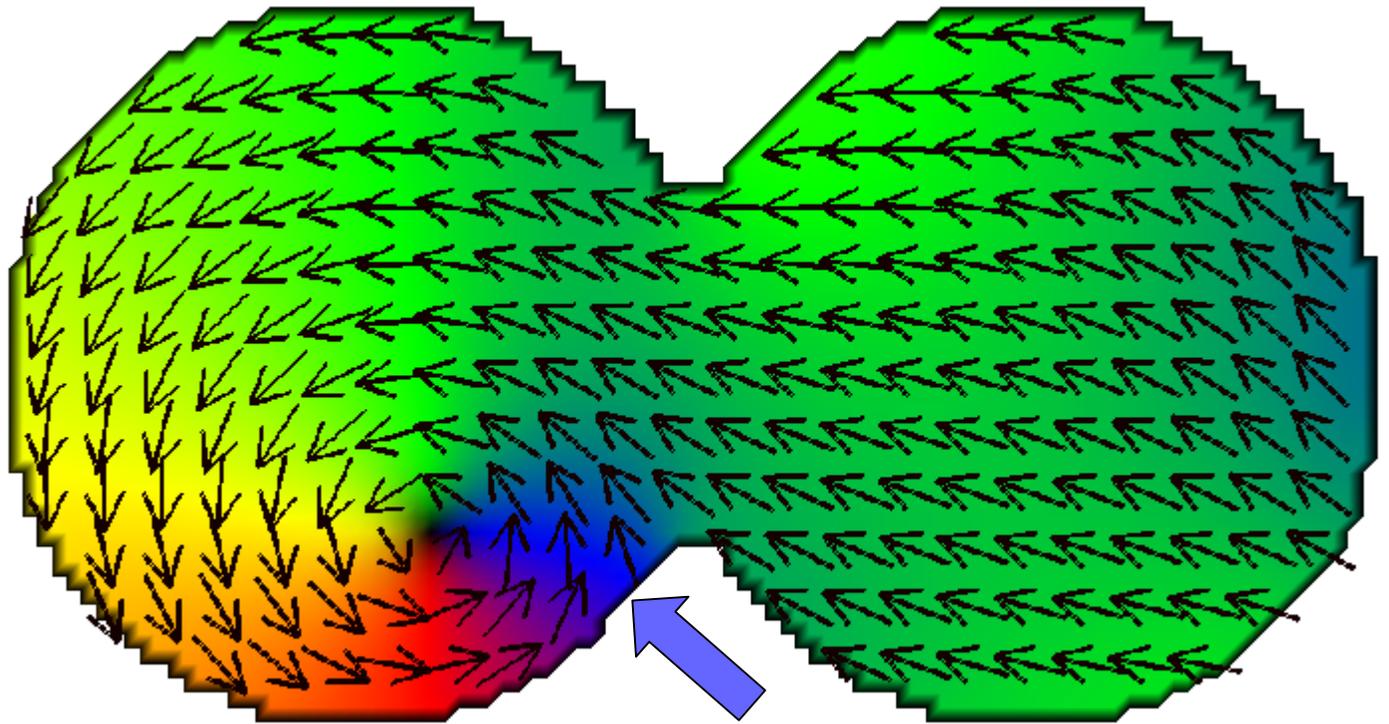
Switching with $H_x=50$ in bias field
 $H_y=50$



Dealing with ultra-thin film systems with multiple ground states.

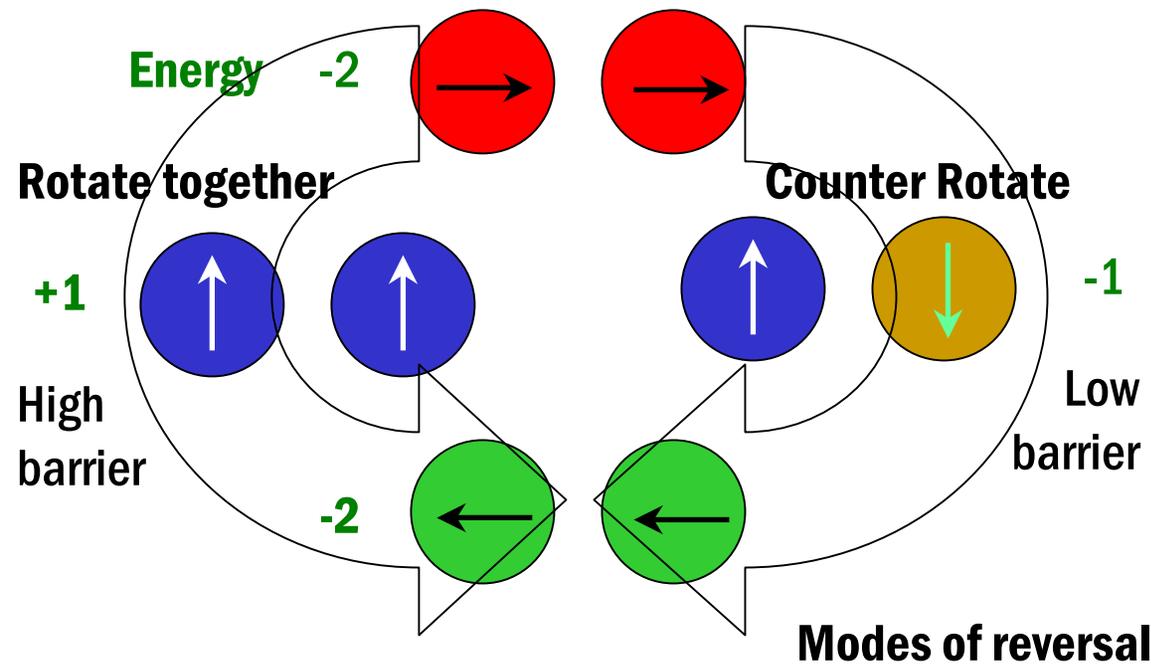
Hysteron, overlapping circles, and Brown's paradox.

(low field switching without thermal problems)

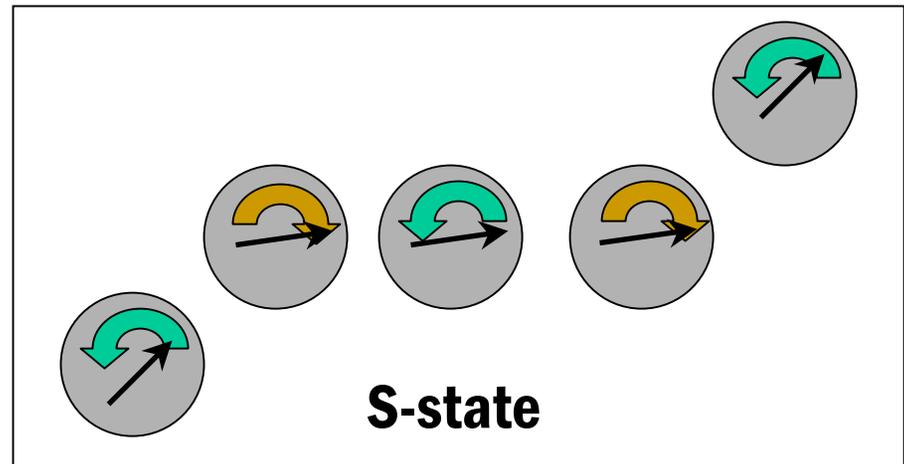
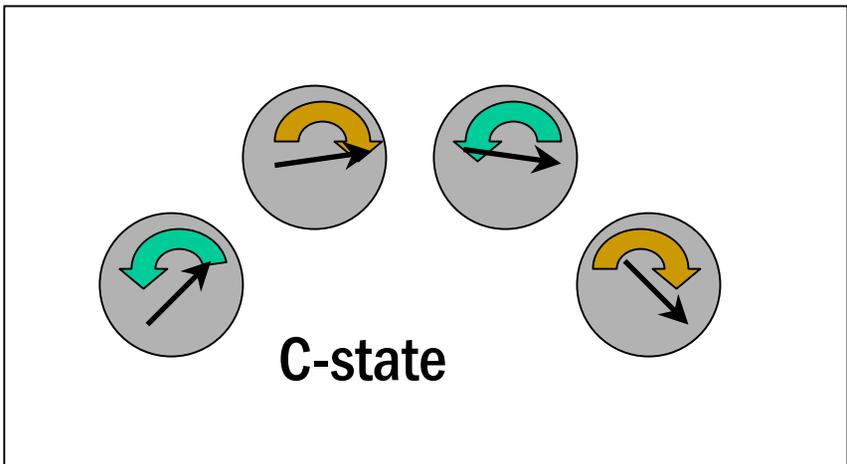


The hysteron in zero field.

The wall used
in reversal is
hiding here.



←
Apply field H to the left



The response function of interest is generally called the switching astroid, the dependence of the minimum switching field, H_{xs} , on the bias field, H_y . For the ideal uniform-rotational response, associated with the term Stoner-Wolffarth particle, the switching is the four-cusped hypercycloid known as the astroid,

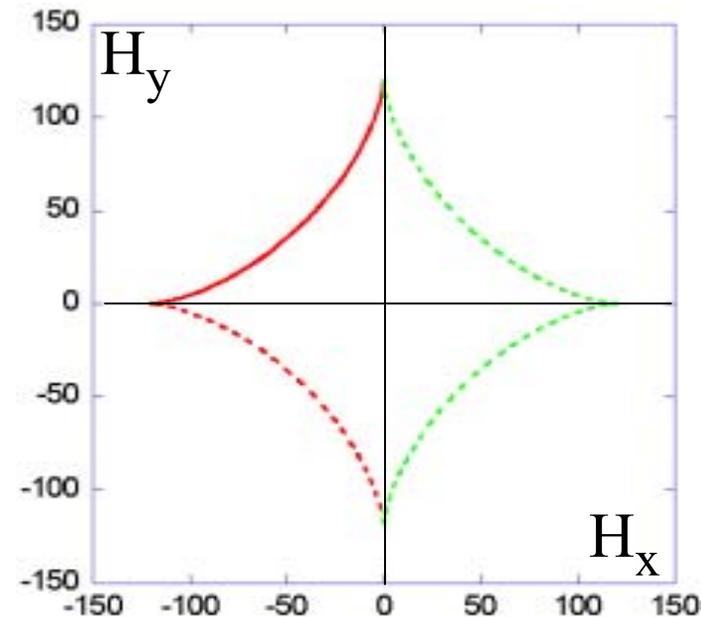
$$|H_{xs}/H_k|^{2/3} + |H_y/H_k|^{2/3} = 1.$$

A bit switching by a different mode has a different switching astroid. The differences in the asterooids can exceed the six-sigma

deviation for the ensemble with all bits switching in the same model.

It is a common experience that the same bit will switch within a small range of fields, determined by temperature fluctuations, for a hundred cycles and then suddenly switch at an entirely different field because the thermal fluctuations have triggered a different switching mode.

The selectivity problem becomes one of mode selection.

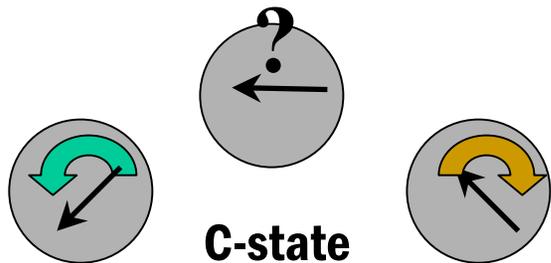


The idea is to have a ground state that does not switch under either the word field or the digital field alone, that is, if any field is applied along either of the axes and then removed, the bit returns to its original state.

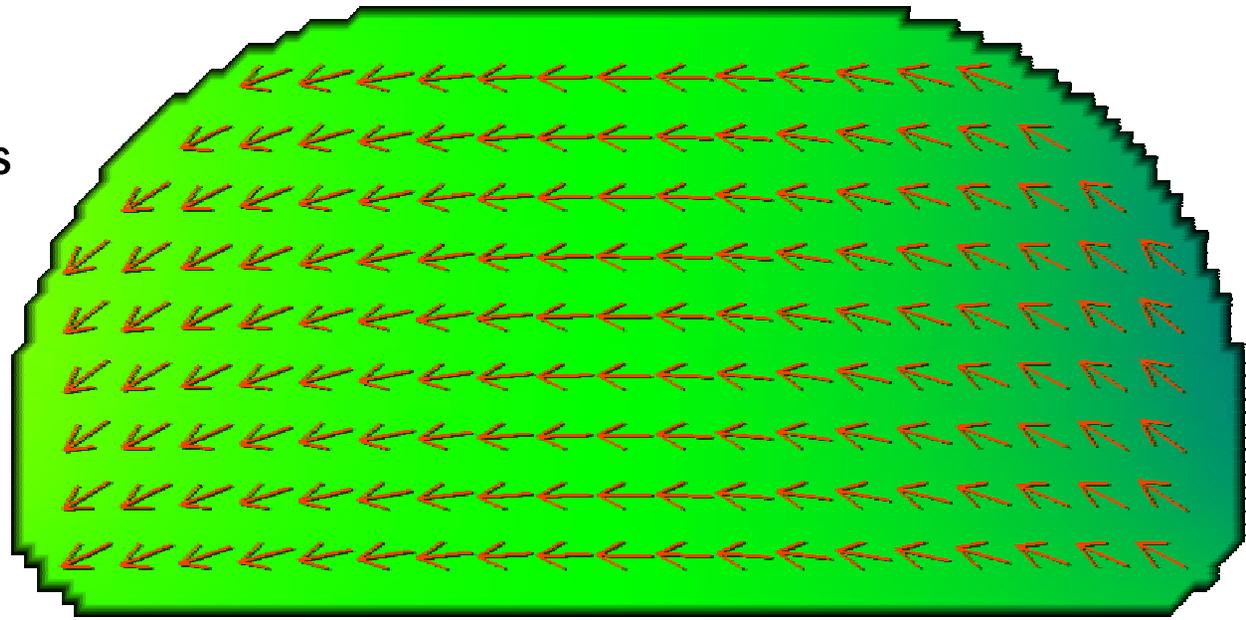
But if the digital field is above a threshold it “unlocks the door”. Then there is a suitable word field, which will switch the bit, which reaches its opposite ground state on removal of both fields.

There is still a switching diagram reminiscent of the astroid, except now there is the caveat that this holds only when the bias H_y exceeds a threshold.

This is achieved by choosing a shape for the bit that has as a ground state known as the “C-state”.

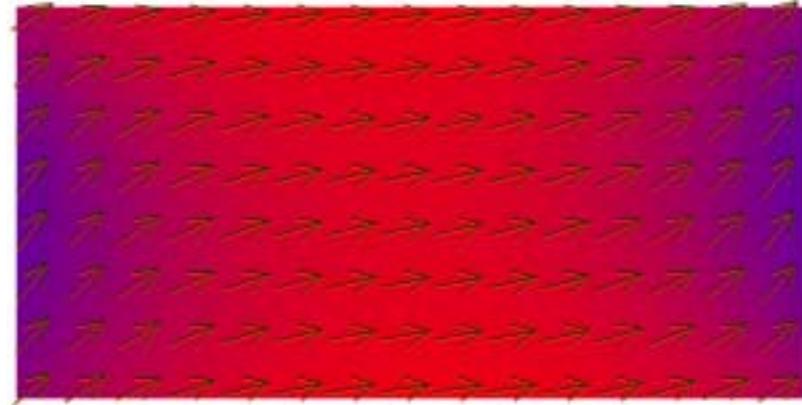


C-state

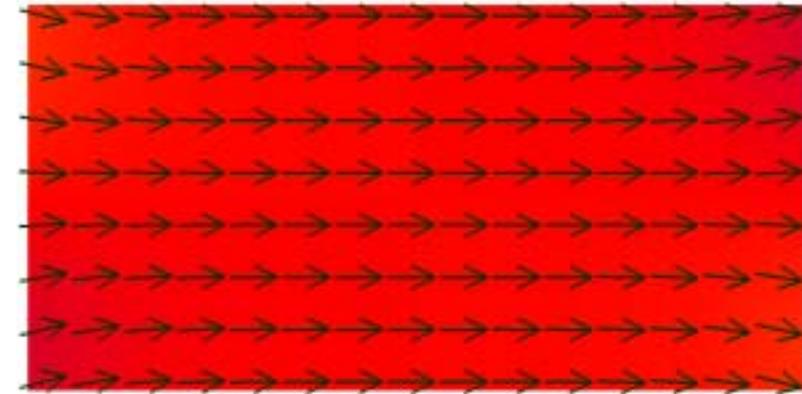


The C-state solution

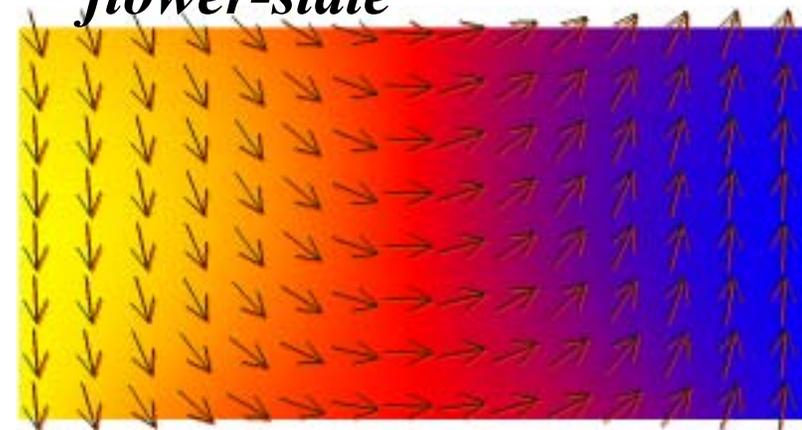
The terms C-state and S-state arise from consideration of elements with blunt ends, epitomized by the rectangular shape. The intermediate state is sometimes referred to as the flower state. The S-state and C-state are almost degenerate in energy, with the flower state representing the barrier between the two lower energy states. The S-state can be achieved by applying a bias field using the digital line. The C-state can be achieved by thermal activation or sample imperfection when reducing an applied field along the length of the rectangle. To force the C-state on the rectangle would require a gradient field.



S-state



flower-state



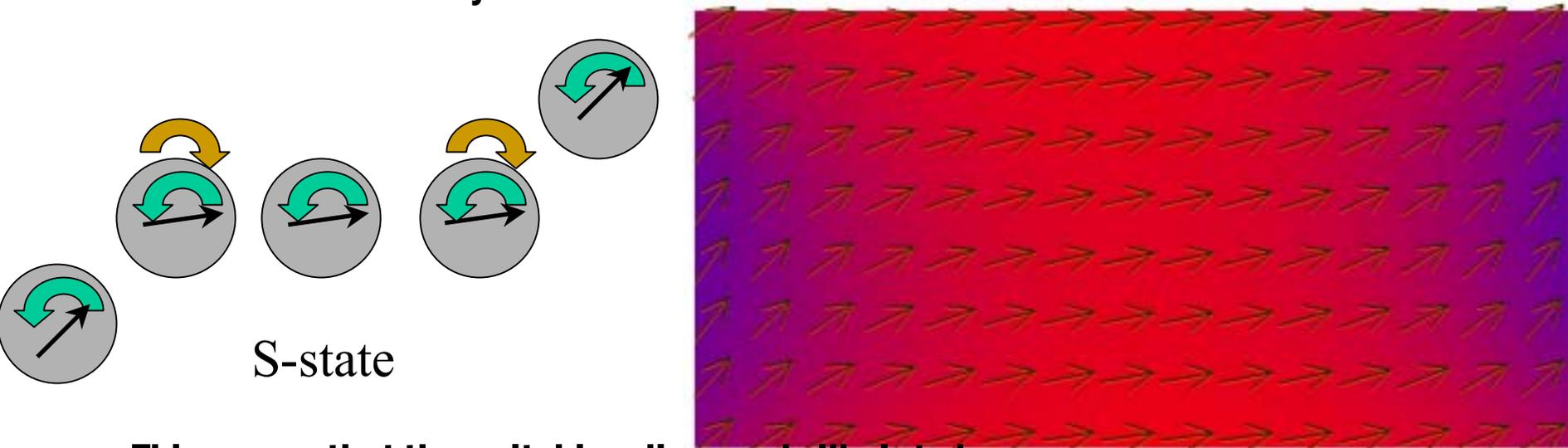
C-state

The S-state mode in a rectangle can be guaranteed if the digital-line field is removed after the word-line field is removed.

There are two problems with the S-state mode.

It may not be stable when a switching field is applied, in either direction, without the bias field.

The S-state is already biased.

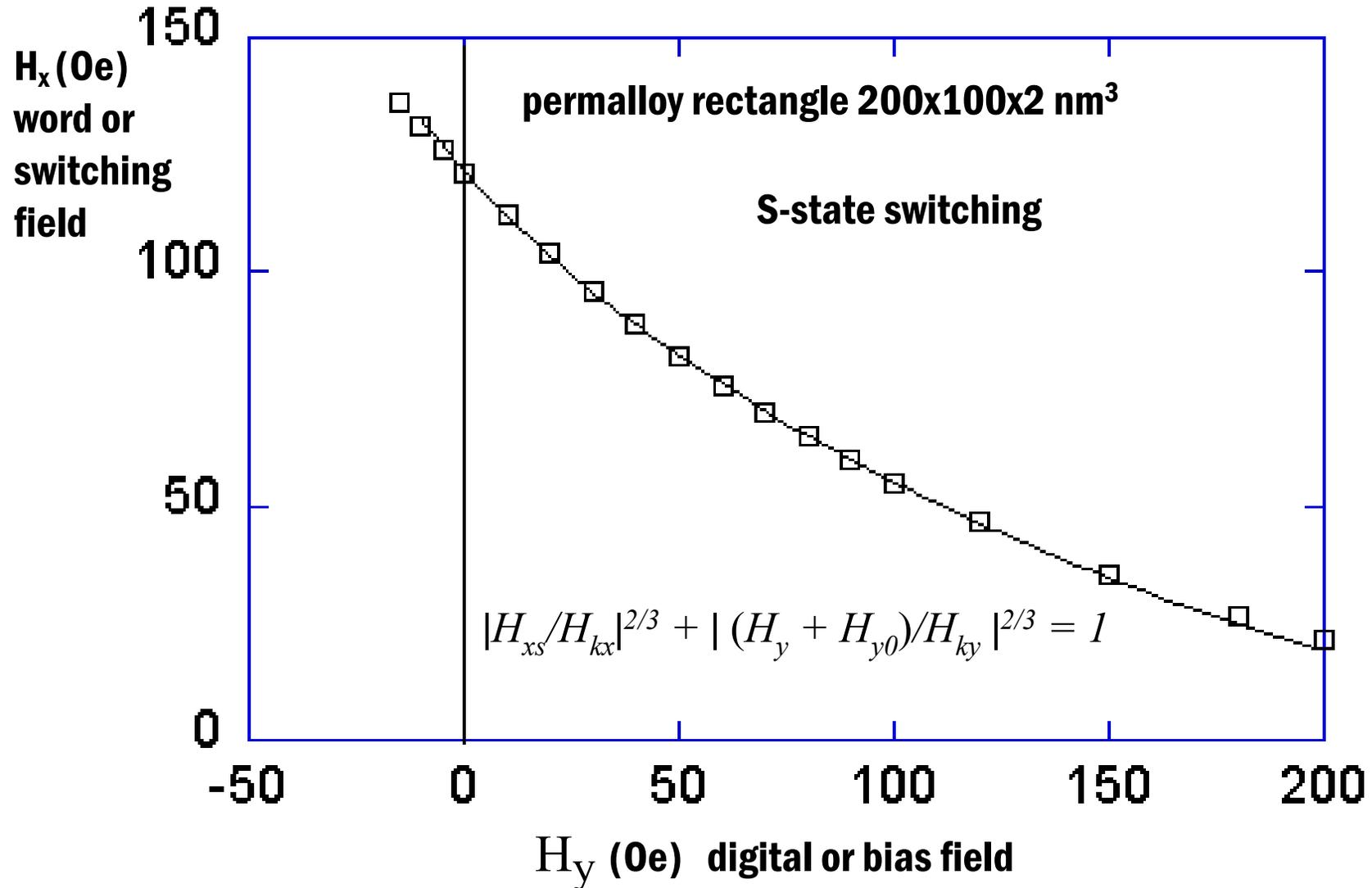


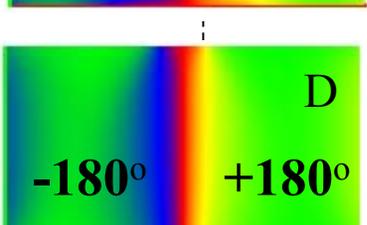
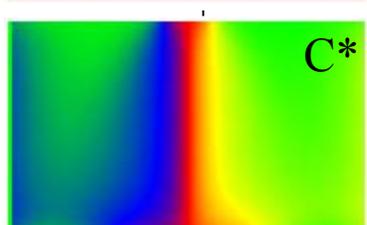
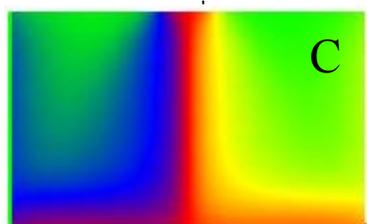
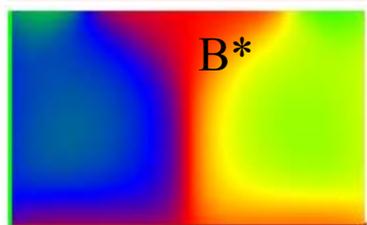
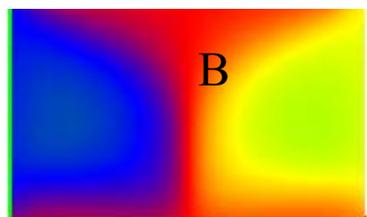
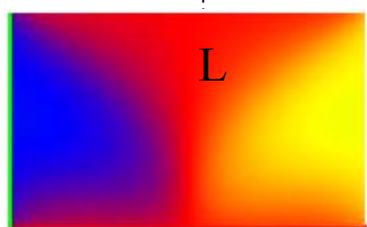
This means that the switching diagram is likely to be

$$|H_{xs}/H_{kx}|^{2/3} + |(H_y + H_{y0})/H_{ky}|^{2/3} = 1,$$

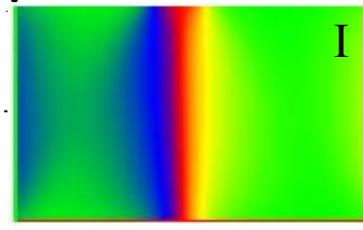
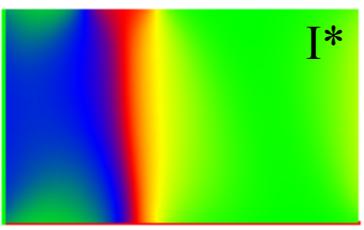
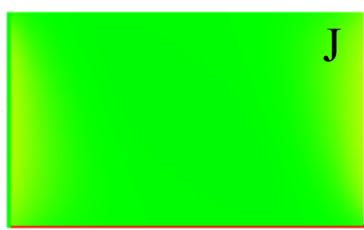
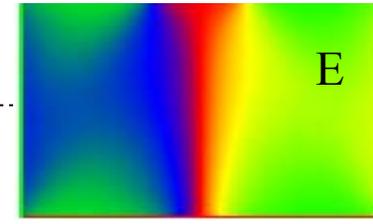
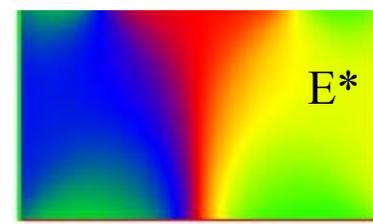
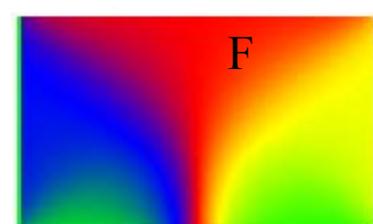
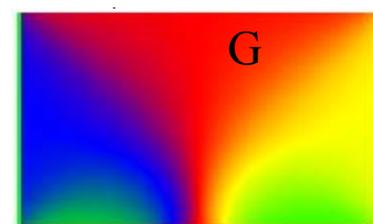
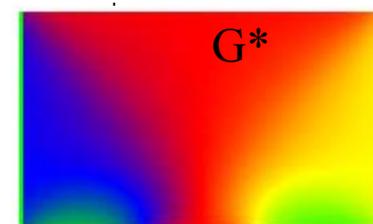
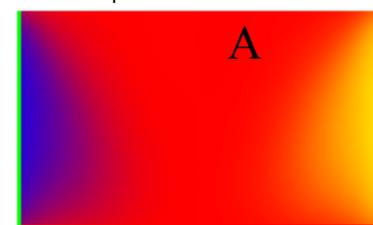
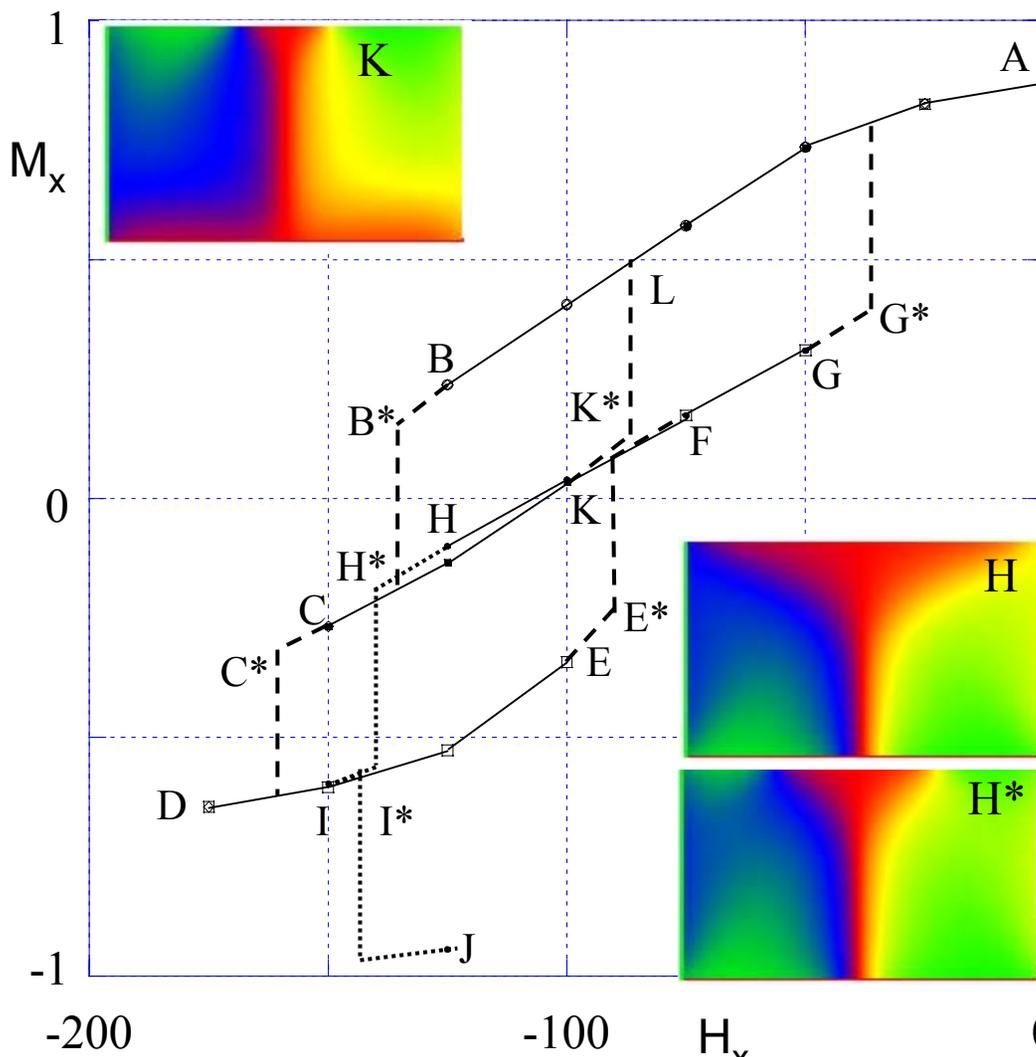
where H_{y0} is the effective bias field coming from the shape of the bit, and the H_x and H_y fields are no longer on equal footing.

The calculated equilibrium switching astroid for a rectangular bit in the S-state is shown for the dimensions 200x100x2 nm³, which is compatible with state-of-the-art silicon technology in size and switching fields.



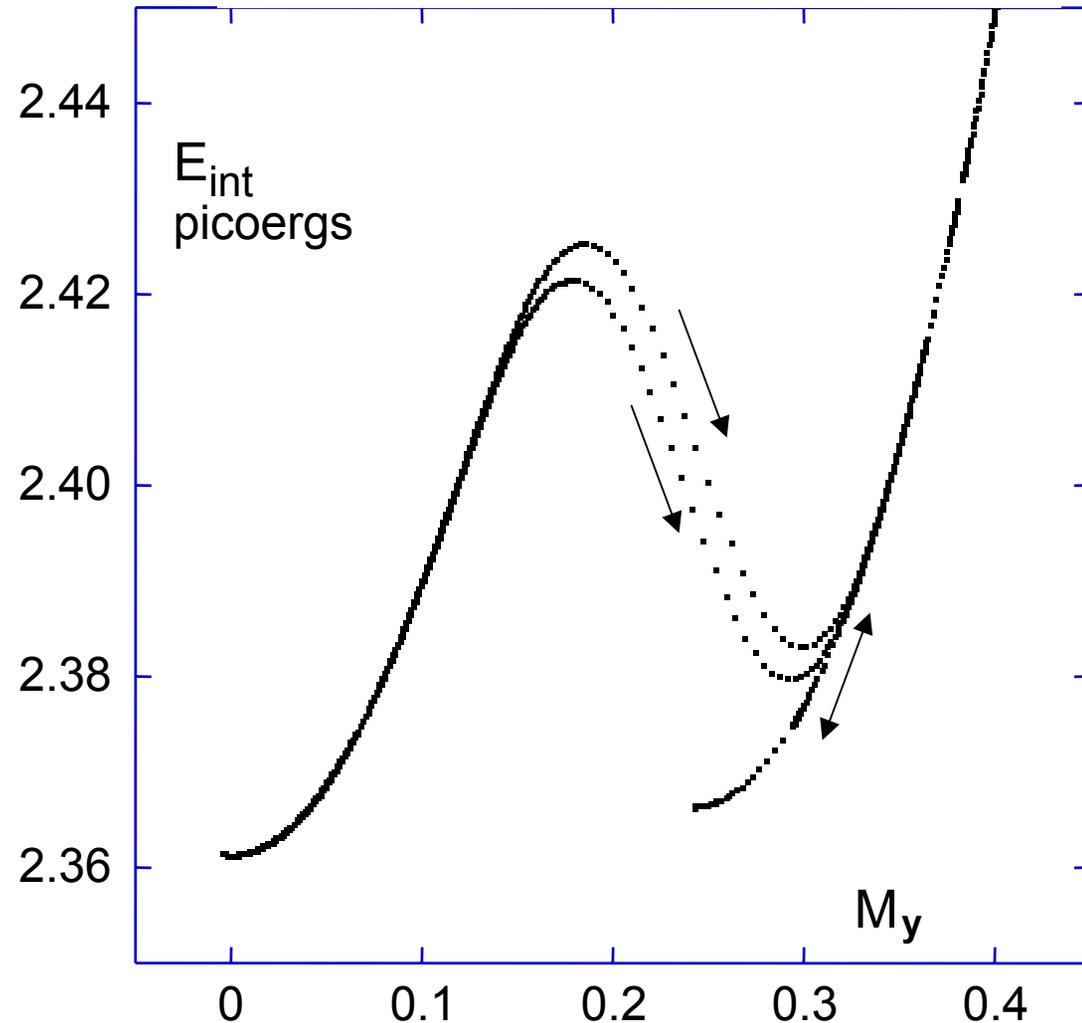


C-state switching in a rectangle



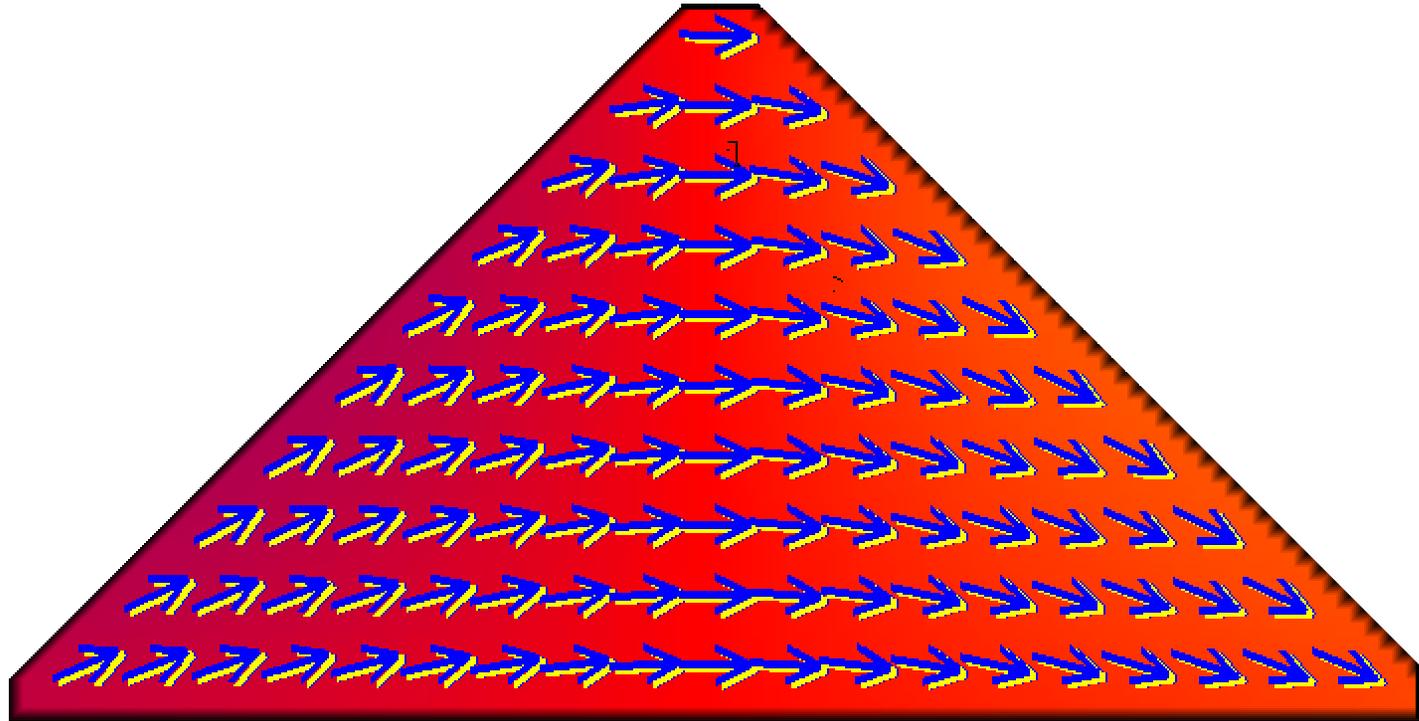
To switch from the C-state to the S-state for this bit requires a bias field $H_{ys} = 17.5$ Oe. There is an energy barrier between the two states which can be estimated by assuming that any switching will take the same path in configuration space as occurs when the switching is caused by the application of the field.

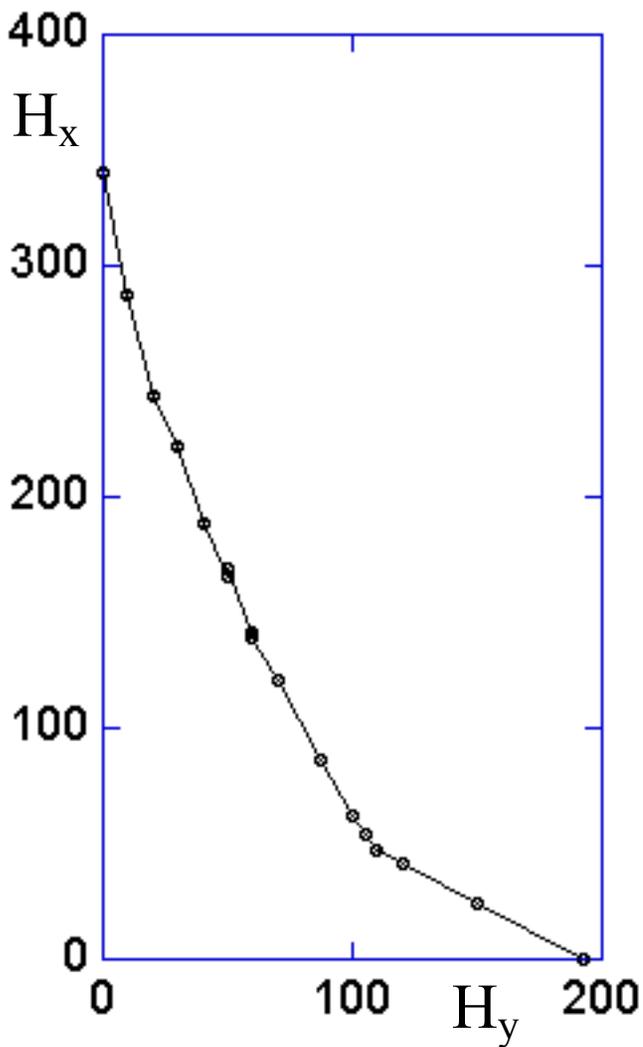
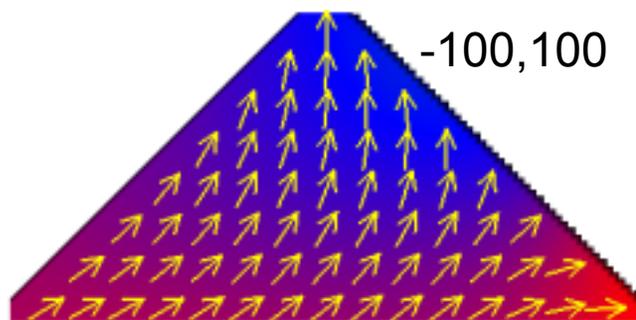
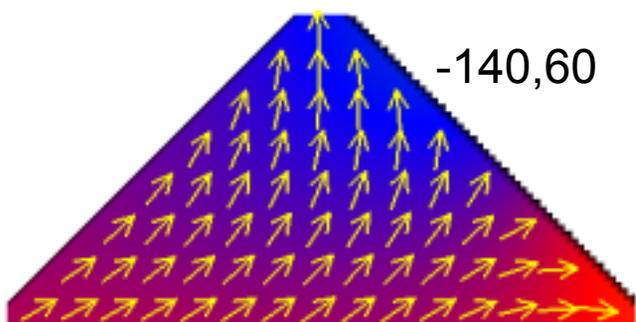
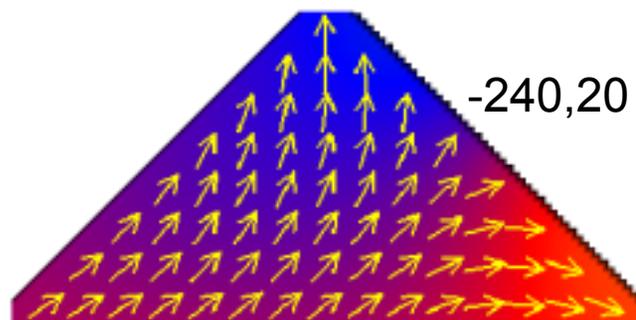
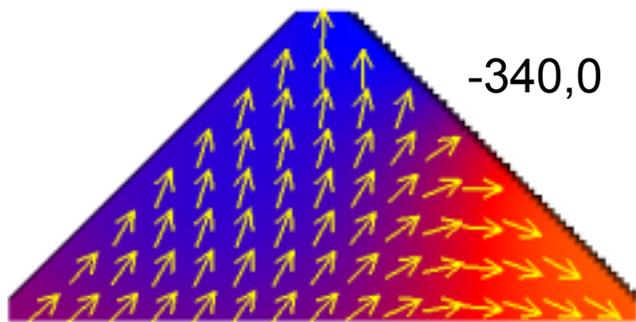
One just calculates the energy at each point on that switching trajectory and subtracts the contribution from the Zeeman term. This may be called the internal energy E_{int} . E_{int} as a function of the configuration can be expressed in terms of $\langle m_y \rangle$, as shown here, or in terms of an effective angle $q = \arctan(\langle m_y \rangle / \langle m_x \rangle)$.



The remedy promoted here is to shape the bit so that it always drives to the C-state after any field is removed and thermal activation between the C-state and the S-state is suppressed. This is achieved by breaking the up-down (on the page) symmetry of the bit to make the C-state preferred.

The C-state becomes the lower energy state and the S-state becomes unstable under a trapezoidal distortion of the rectangular shape. The extreme limit of this is to use the triangular shape.

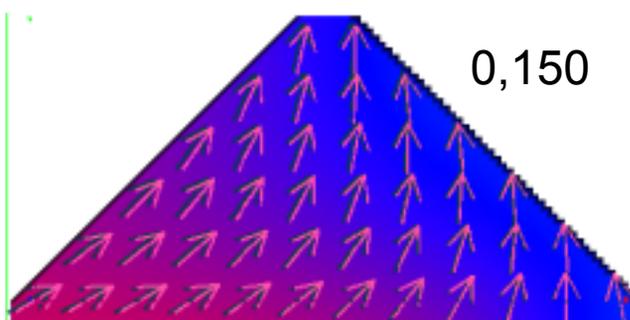


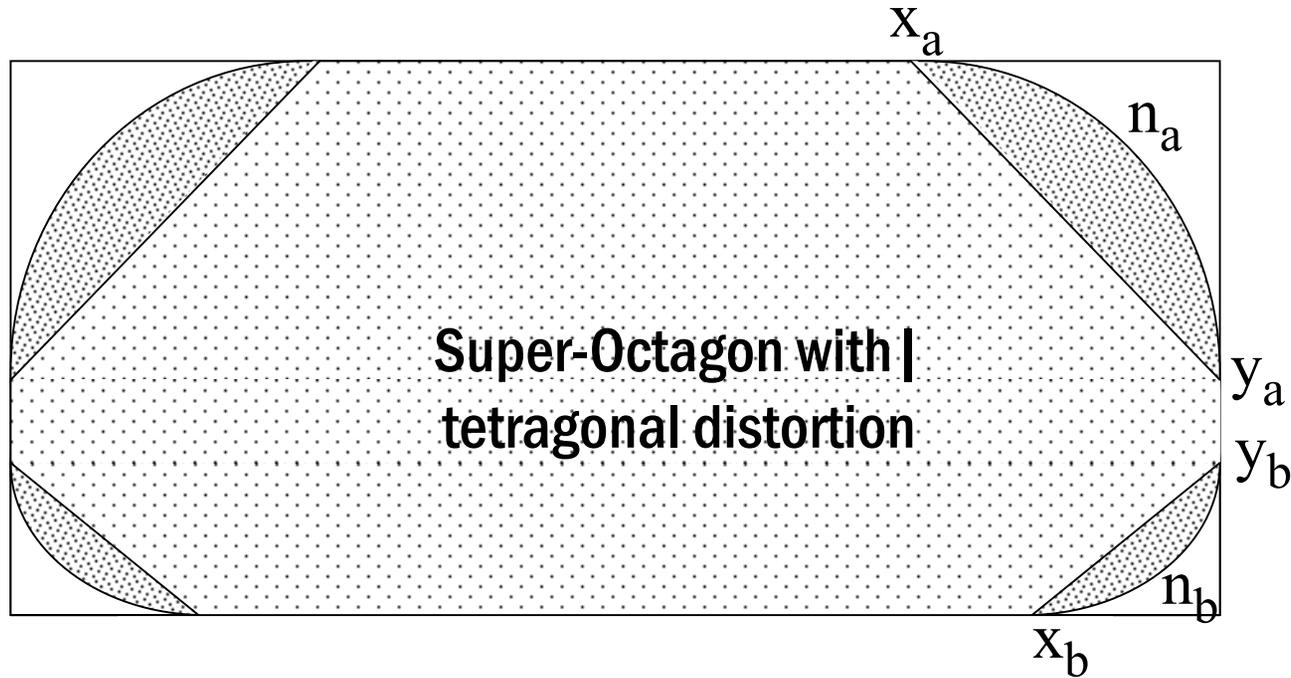


**Switching astroid
for triangular bits.**

200x100x2 nm³

**Word field applied
to the left**



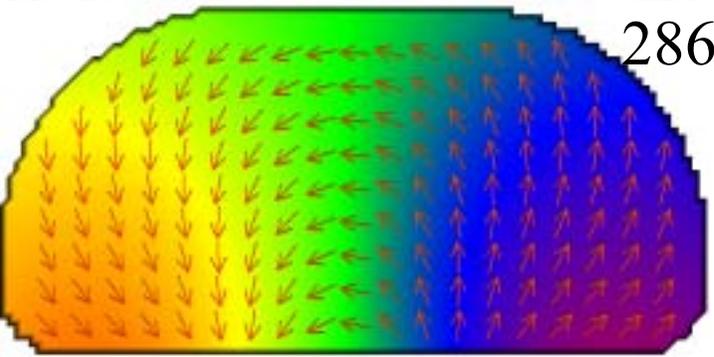
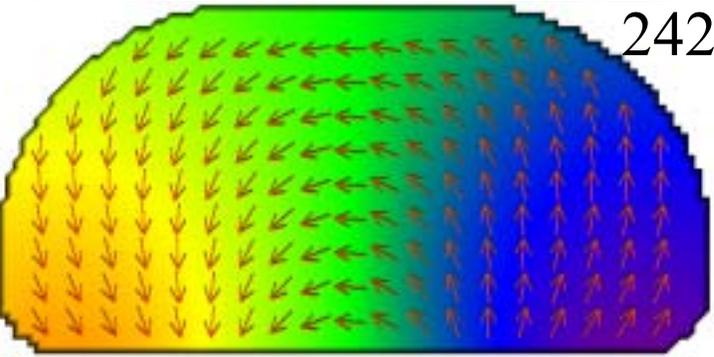
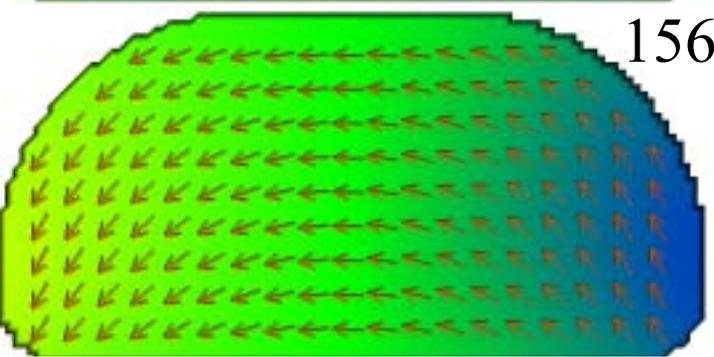
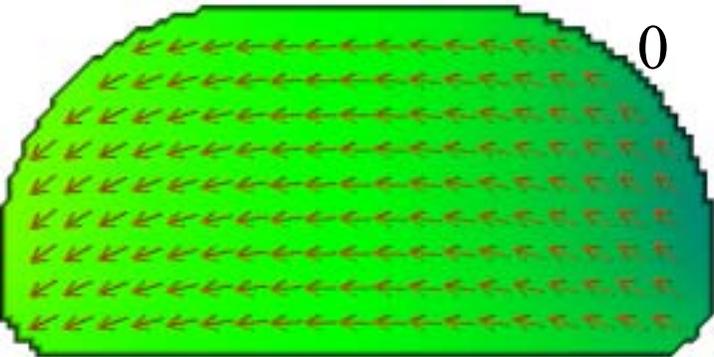


To investigate a range of possible shapes it is useful to introduce the super-octagon, which is characterized by a thickness t , width w and length L , plus six additional parameters.

The super-egg formula $|x/x_0|^n + |y/y_0|^n = 1$ generalizes the ellipse ($n=2$) to include the rectangle ($n=\infty$) and the diamond ($n=1$).

The super-octagon with trapezoidal distortion has super-egg-quadrants for each of its four corners with parameters x_a , y_a , and n_a for the upper two corners and parameters x_b , y_b , and n_b for the bottom two corners.

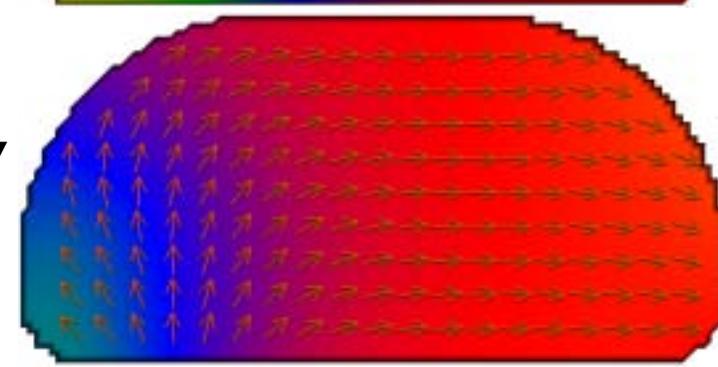
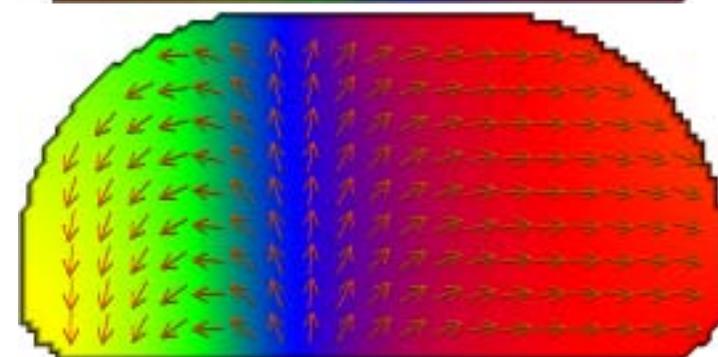
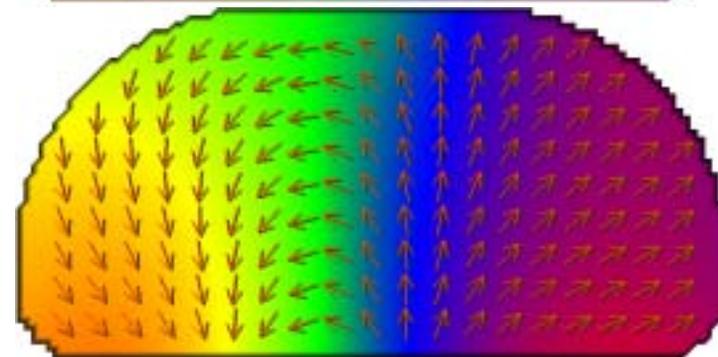
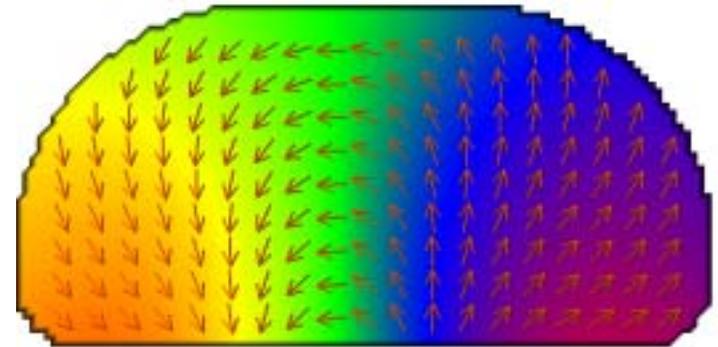
The super-octagon is now built into Scheinfein's LLG.



stable to 310 Oe

Time at
310 Oe

H_x



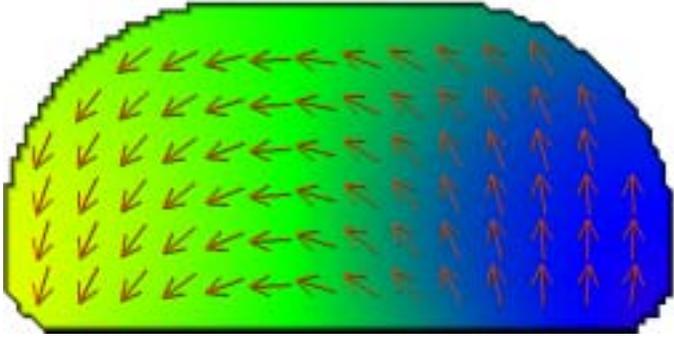
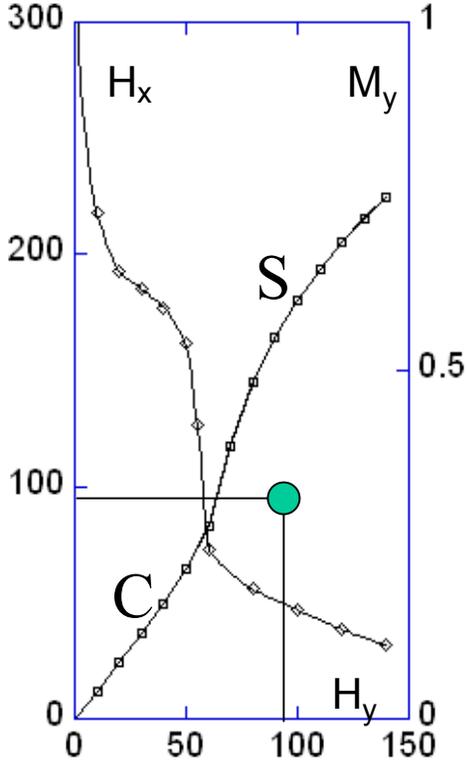
C-state stability
of the tetragonally
distorted
super-octagon

$200 \times 100 \times 2 \text{ nm}^3$

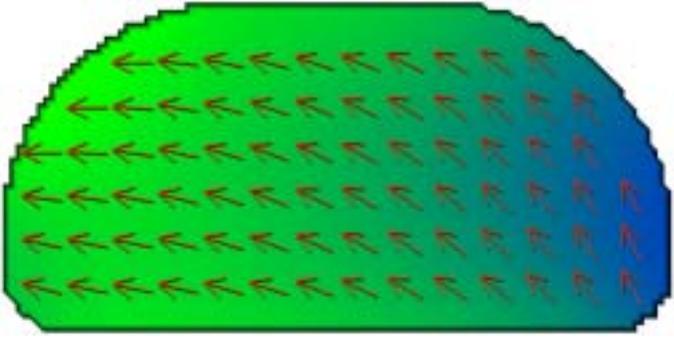
0.6, 1.5, 1.92, 2.1 ns

Configurations of the standard super-octagon at the critical moment of irreversibility along the switching astroid for the values of H_x , H_y as indicated. If the fields were infinitesimally less, it would take a thermal fluctuation to initiate the irreversible switching.

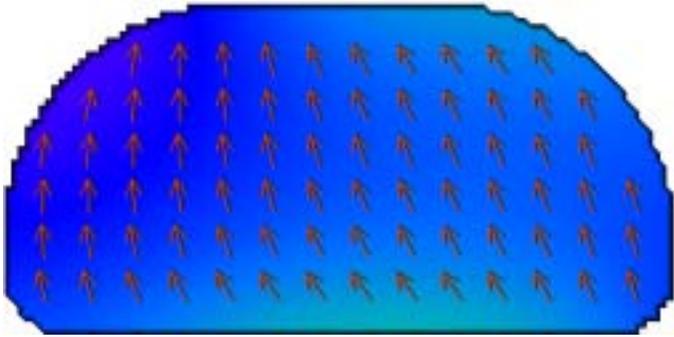
H_x is applied to the right.



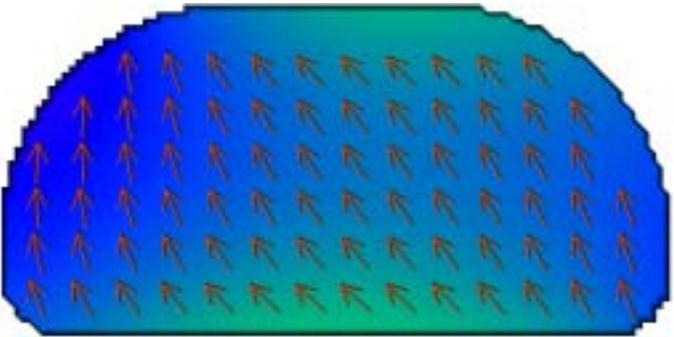
217.68, 10



73.25, 60

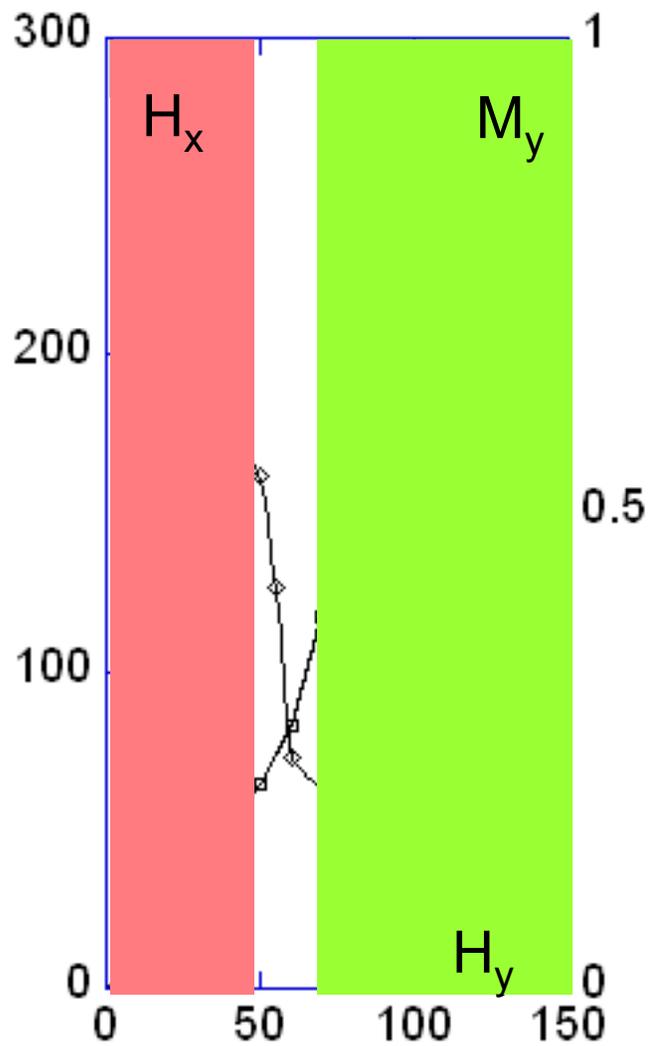
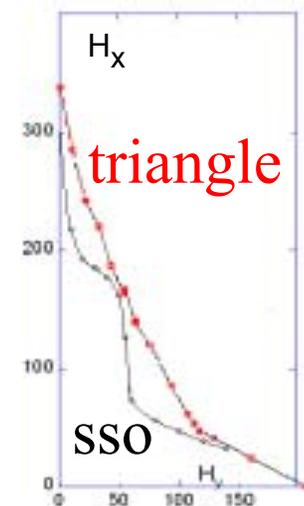


31.78, 140

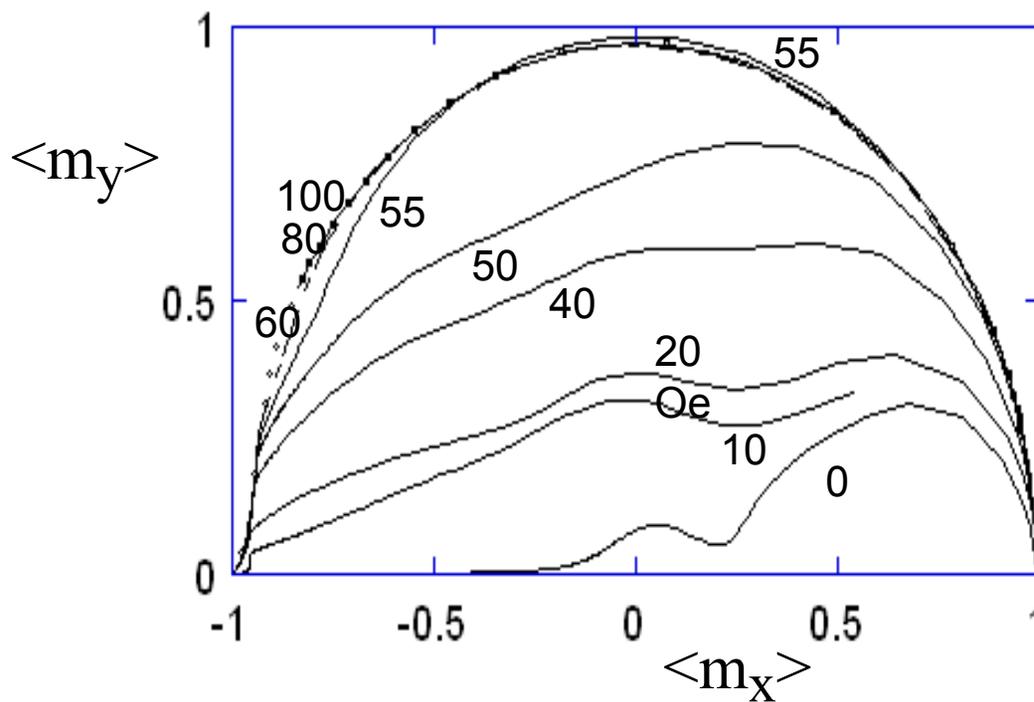


55.83, 80

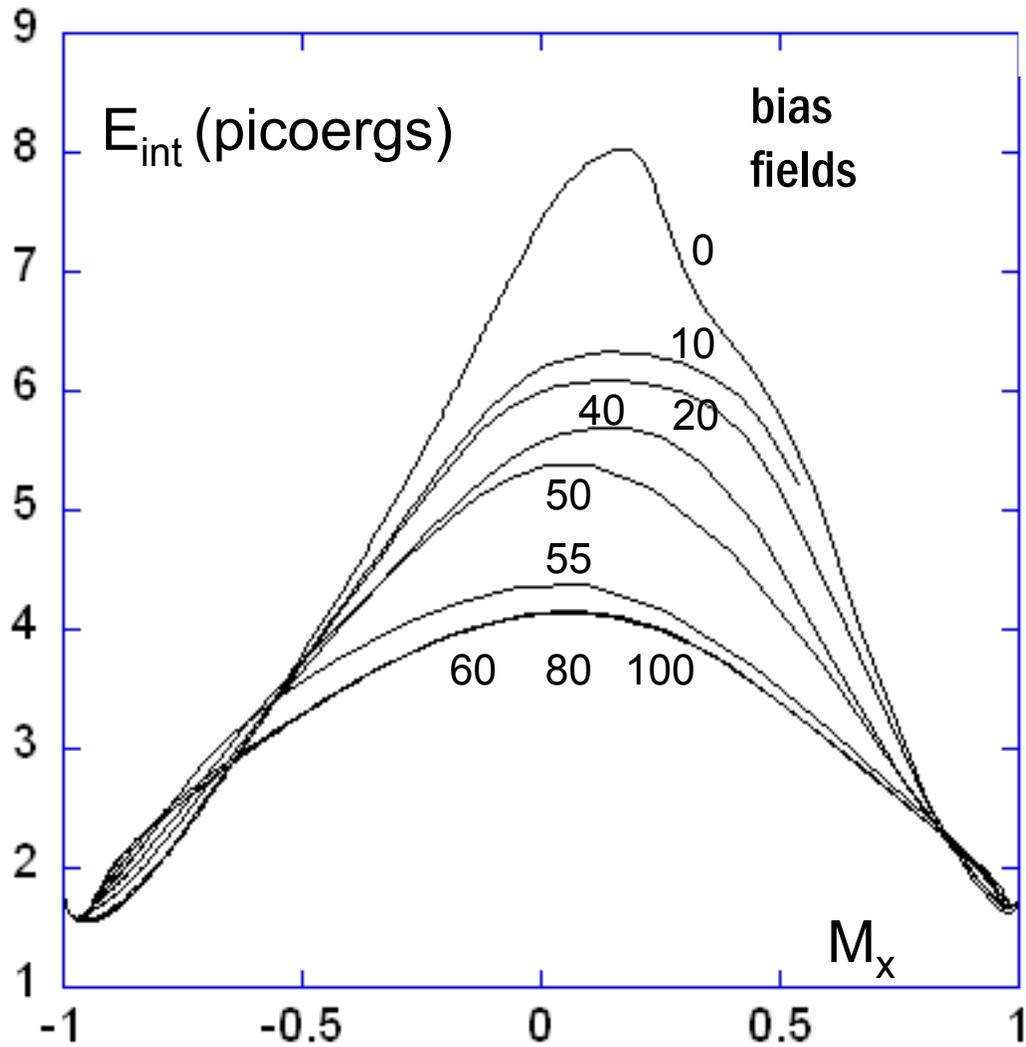
For low bias fields the C-state is “locked”
 For high bias fields, uniform rotation like S-state



Switching paths in $\langle m_x \rangle, \langle m_y \rangle$ space



The internal energy barrier is large



Motorola Sets Major Milestone with 1 Mbit MRAM Universal Memory Chip with Copper Interconnects

*On Track for Full-Scale Production by 2004;
Huge Consumer Benefits on the Way for Cell Phones,
Mobile Devices, Laptops, PCs and Automobiles*

HONOLULU – June 10, 2002 –

Motorola's Semiconductor Products Sector (SPS) in collaboration with Motorola Labs is unveiling the first 1 megabit (Mbit) MRAM universal memory chip at the 2002 VLSI Symposia on Technology and Circuits.

Motorola Sets Major Milestone

This significantly advances the state of research in universal memory, bringing the technology closer to revolutionizing the semiconductor memory market.

“MRAM has the potential to become the prevalent memory of choice for the vast majority of digital consumer applications like cell phones, mobile devices, laptops, PCs and even automobiles,”

said Saied Tehrani, director of MRAM technology at SPS.

“As leaders in developing this technology, we are solidly on track to achieve our goal of MRAM samples in 2003 and production in 2004.”

Mark Twain dancing dog.

The biggest problem facing MRAM is the competition.

DRAM (Never bet against 50 years of engineering.)

**Ferro Electric Random Access Memory FERAM
(break through in solving the fatigue problems)**

Flash Memory (From the diode to the pentode lowers the barriers.)

**Newsflash 9/16/02 Cypress Semiconductor, Micron and
Infineon**

**announce a consortium to produce CellularRAM, now,
PseudoStaticRAM 32 Mb devices**

128 Mb by Fall 2003

Colossal Magnetoresistance

(Who knows what new materials will be found?)

Spintronics (leaving the realm of science fiction)

(The nuclear spins remember for days.)

Can the storage industry benefit from the work in MRAM?

Maybe.

Try using pairs of pixels as the ultimate unit of storage.

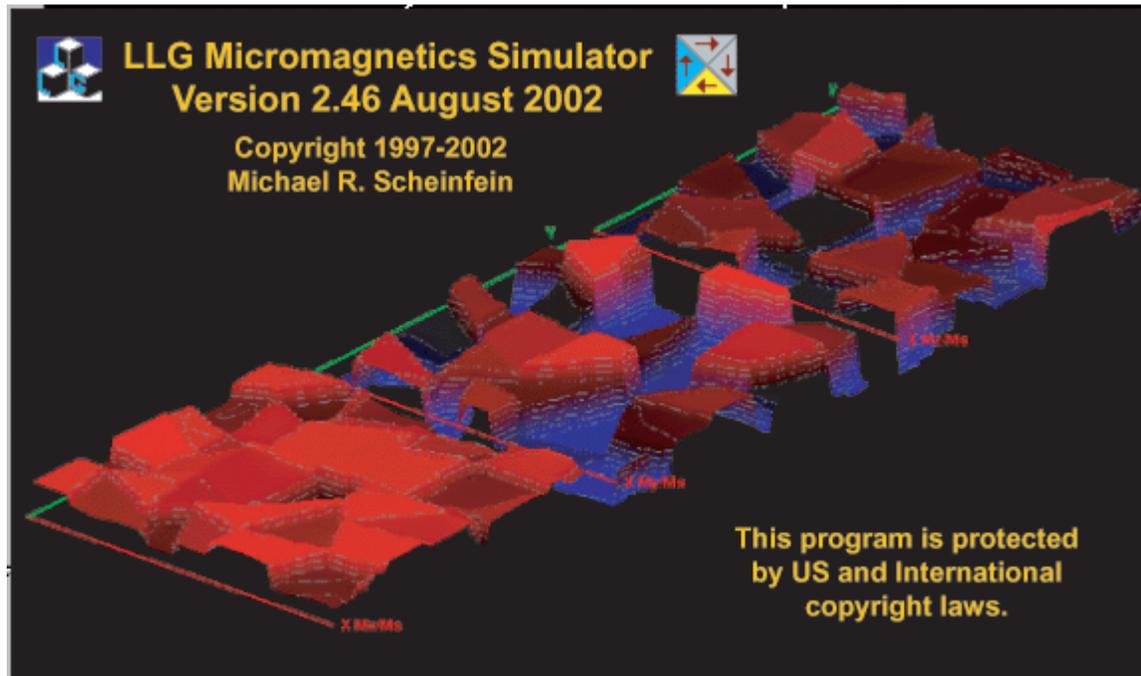
Micromagnetics

Anthony Arrott

Center for Interactive Micromagnetics, Virginia State University, USA

Professor Emeritus, Simon Fraser University, Canada

Guest Scientist, National Institute for Standards and Technology, USA



With special thanks to Bretislav Heinrich and Michael Scheinfein at Simon Fraser University.