An Advanced High Speed Solid State Data Recorder

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Corporation Overview

- Founded in 1986
- Headquarters in Austin, TX
- Professional Staff of Scientists & Engineers
- Capabilities
  - Systems Engineering
  - Electrical/Mechanical Design
  - ASIC Design
  - Prototype & Test Labs
  - Software Development
**Capture Ultra High Speed Data Sources**
- Video (1024 x 1024 pixel x 1000 frames/s)
- Multiple independent data sources
  - 1 - 32 channels of 1 - 10 bit data at 50 MHz

**Capture PCI Compatible Data Sources**
- SCSI, Fibre Channel, Ethernet, DCRsi™, 1553B
- Custom instrumentation interfaces

**Flight Applications**
- Size constrained applications (e.g. pod mount)
- Environment constrained applications (e.g. high ‘g’
SPEC

Architecture

- **SCSI**
- **DCRs™**
- **Fibre Channel**
- **Ethernet**

**Recorder Controller**

**High Speed Interface**

**Camera Interface Adapter**

**Memory Bus**

- 32-bit 33 MHz
- 256-bits 66 MHz

**Memory Module**

**Camera**

32 ≤10-Bit Independent High Speed Inputs
High Speed Interface

1 - 10 Bit Data Words with Independent Controls

32KB Data Buffers
Lossless Compression
Error Correction Coding
Packetization (Time Stamp)

Packet Arbitration
Packet Data Buffers
256 Byte Data Packets

256 Bit 66 MHz Bus

DATA TRANSPOSER (FPGAs)

MEMORY BUS

CTRL DATA

ASIC #1
ASIC #2
ASIC #3
ASIC #32
SPEC

High Speed Interface ASIC
**SPEC**

**ASIC Specifications**

- **Input Data**
  - Variable 1 -10 Bit Data Words
  - 50 MHz Maximum Sample Rate
  - Clock and Data Ready
  - 32K Word Data Buffer

- **NASA USES Lossless Compression Algorithm**

- **CCSDS Compatible Packetization**
  - Header + Data + ECC
  - Time Stamp
  - Reed-Solomon Forward Error Correction Coding

- **Implemented in 0.5 micron CMOS Technology**
SPEC Recorder Controller

- **Programmable Controller**
  - Embedded Processor with Firmware
  - Bi-directional Interface to 256-Bit Memory Bus
  - PCI Bus Master

- **Industry Standard PCI Bus Interface**
  - SCSI
    - Standard PC Device Driver
    - Internal Tape Module Backup Capability
  - DCRsi™
  - Fibre Channel
  - Ethernet
  - Carrier with Industry Pack (IP) Modules
Three Memory Configurations

- **High Speed Memory**
  - SDRAM Modules
  - High Performance, High Capacity, Low Cost
  - Requires Battery Backup for Nonvolatile Storage

- **High Speed Memory with Nonvolatile Backup**
  - SDRAM & EEPROM Modules
  - High Performance, Less Capacity, High Cost
  - SDRAM contents transferred to EEPROM after capture

- **Low Speed Nonvolatile Memory**
  - EEPROM Modules
  - Low Performance, High Capacity, Low Cost
**SPEC**

Typical Operation

- **Capture 10 - 20 s of High Speed Data (e.g. Video)**
  - Compress 2:1 on average, ~7:1 maximum
  - Packetize compressed data
  - Store in SDRAM

- **Data Retrieval**
  - Controller reads data over 256-Bit Memory Bus
  - Controller uncompresses/error corrects/formats data
  - Controller transfers formatted data over PCI bus
    - SCSI to tape backup or PC
    - DCRsi™ to tape backup
    - Ethernet to workstation
Data Storage Formats

- Data stored in compressed or uncompressed format
- Compressed data packets stored in non-sequential order (packets written to memory when complete)
  - Maximum storage capacity
  - Fast sequential access
  - Slower random access (packet search required)
- Uncompressed data packets stored in sequential order
  - Less storage capacity
  - Fast sequential access
  - Fast random access
<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chassis</td>
<td>ATR Short (Long Option)</td>
</tr>
<tr>
<td>Weight (without memory)</td>
<td>≤18 lbs</td>
</tr>
<tr>
<td>Max Memory Modules</td>
<td></td>
</tr>
<tr>
<td>- 1 ATR Short</td>
<td>5 modules (15 GB)</td>
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<tr>
<td>- 1 ATR Long</td>
<td>9 modules (27 GB)</td>
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<tr>
<td>Memory Module</td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td>≤2 lbs</td>
</tr>
<tr>
<td>Capacity</td>
<td>3 GB (with 64 Mbit TSOPs)</td>
</tr>
<tr>
<td>Memory Type</td>
<td>SDRAM or EEPROM</td>
</tr>
<tr>
<td>Cooling</td>
<td>Conduction</td>
</tr>
<tr>
<td>Environment</td>
<td>Flight</td>
</tr>
<tr>
<td>Data Rate</td>
<td></td>
</tr>
<tr>
<td>High Speed (sustained)</td>
<td>10.4 Gbps</td>
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<tr>
<td>High Speed (burst)</td>
<td>16 Gbps (32 ch x 10-bit x 50 MHz)</td>
</tr>
<tr>
<td>Low Speed Data/Control</td>
<td>1 Gbps (PCI 32 bit x 33 MHz)</td>
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System Architecture Complete

Interface Specifications Complete
- High Speed Interface
- Wide Bandwidth Memory Bus
- PCI Interface

High Speed Interface
- ASIC ready for fabrication
- Transposer FPGA design complete

Alpha Unit Complete in August
- ATR Short Chassis with Power Supply & Backplane
- Controller with DCRsi™ Interface
- Memory Module (16 Mbit SDRAMs)