MRAM: Device Basics and Emerging Technologies

Matthew R. Pufall

National Institute of Standards and Technology
325 Broadway, Boulder CO 80305-3337
Phone: +1-303-497-5206   FAX: +1-303-497-7364
E-mail: pufall@boulder.nist.gov

Presented at the THIC Meeting at the National Center for Atmospheric Research, 1850 Table Mesa Drive, Boulder CO 80305-5602
July 19-20, 2005
Collaborators:

**NIST:**
- Bill Rippard
- Shehz Kaka
- Steve Russek
- Tom Silva

**Hitachi Global Storage:**
- Jordan Katine

**Freescale:**
- Fred Mancoff
- Nick Rizzo
Outline

• What is MRAM? What are its advantages?
• When will we see MRAM?
• How does MRAM work?
  • Spintronics basics: Electron spin and Magnetoresistance
  • Anatomy of an MRAM bit
  • Magnetic Switching
• Engineering Challenges: Consistency and Thermal Stability
• Freescale’s MRAM solution: “Toggle” MRAM
• Big Problems in the Nano-Future: Scaling of bits
• Emerging Solutions to Scaling: Spin Torque Switching
What is MRAM?

**Magnetic-based Random Access Memory:**

Uses small magnetic element to store {1,0} rather than electric charge

(Some) **Other types of RAM:**

<table>
<thead>
<tr>
<th>Storage Method</th>
<th>Virtues</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM Charge on capacitor</td>
<td>speed, size, cost</td>
</tr>
<tr>
<td>SRAM Multiple transistors</td>
<td>speed, size, no refresh</td>
</tr>
<tr>
<td>FRAM Ferroelectric capacitor</td>
<td>nonvolatile, speed</td>
</tr>
<tr>
<td>Flash Transistor w/ extra isolated gate</td>
<td>nonvolatile, cost, size</td>
</tr>
</tbody>
</table>

...All have advantages/tradeoffs: **No “universal” solution**
### MRAM advantages:

<table>
<thead>
<tr>
<th>Feature</th>
<th>Advantage</th>
</tr>
</thead>
</table>
| Nonvolatile              | Data don’t need refreshing  
                          • “instant on”, low power  
                          • Data retention >10 yrs |
| Fast                     | Read/write symmetric  
                          • 25 ns (10 ns in demo)  
                          • byte writeable |
| Unlimited cycling        | No “fatigue” after >$10^{16}$ cycles                                     |
| Viability                | Integrated into CMOS process                                             |

…If made (very) inexpensive and scalable, a potential “universal” solution
When (and where) will we see MRAM?

**Freescale:** Demos out to vendors
Shipping product end of 2005/early 2006

**Uses:** Replace battery-backed SRAM
Cell phone/embedded memory

**Others:** IBM—In development
Toshiba/NEC
Cypress, Honeywell: ?

4 Mb chip, 180 nm process
How does MRAM work?

Ferromagnets have hysteresis: Information stored in state $@H = 0$
- Hard disks, tape storage

Magnetic fields used to change direction (state) of $M$
How do you sense state of $M$?

Magnetoresistance (MR): Resistance depends on direction of $M$

How? Electrons also have magnetic moments: Spin

Low Resistance

High Resistance

“Spintronics”
Magnetization Filters $e^-$ Spin:

Electron spins become spin-polarized in direction of $M$: Spin filter

Nonparallel spins scatter more: Higher resistance

$$\Delta R \sim \cos(\theta_M)$$
Sense $M$ by Resistance:

State of $M$ determined by \textit{electrical} measurement:

“Magnetic Tunnel Junction” (MTJ)
Anatomy of an MRAM bit

Digit Line

Tunnel Barrier
Pinned Ferromagnet
Pinning Layer

Free Ferromagnetic Layer

Bit Line

$H_{\text{hard}}$

$M$

$H_{\text{easy}}$

Hard axis field decreases $H_c$

$RA = 10 \, k\Omega \mu m^2$

$H_{\text{hard}} = 0 \, \text{Oe}$

$H_{\text{hard}} = 40 \, \text{Oe}$
**Bit Selection Energetics**

- **Unselected**
- **½-Selected**
  - *Lower barrier*
- **Selected**

\[ E_b \]

- (a) \( H_{easy} = 0 \)
- (b) \( H_{easy} > 0 \) or \( H_{hard} > 0 \)
- (c) \( H_{easy} > 0 \) and \( H_{hard} > 0 \)
Bit Addressing Challenges

MRAM bit

Bits switched/addressed by two fields
Challenge: **Bit-to-bit variations** make choosing proper currents difficult/impractical

Data courtesy Freescale
Freescale’s Solution: “Toggle” MRAM

Program Line 2

Free Tri-Layer
Tunnel Barrier
Pinned Ferromagnet
Pinning Layer

Ferromagnetic layer
Coupling Layer
Ferromagnetic layer

Coupled tri-layer programs more repeatably
How does Toggle work? Timing

Anti-parallel-coupled layers respond differently to fields:

Figure courtesy Freescale
What does Toggle do?

- Moves “1/2 select” error horizon:

Also increases bit volume (& thermal stability)

Data courtesy Freescale
Freescale 4Mb MRAM Layer structure

Program path for Writing information

Program Path: Dashed green line
Sense Path: Red line (isolated)

Chip process at **180 nm node**: Design ported to 90 nm (May ‘05)
## Future Difficulties: Scaling

<table>
<thead>
<tr>
<th></th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DRAM ½ pitch (nm)</strong></td>
<td>100</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>65</td>
</tr>
<tr>
<td><strong>MPU Physical Gate Length (nm)</strong></td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
</tr>
</tbody>
</table>

From ITRS roadmap, 2003

…MRAM must compete with this (aggressive!) scaling to be viable
Scaling Problem: Thermal Stability

As bits get smaller: more susceptible to thermal fluctuations

Energy barrier proportional to volume, anisotropy: Must increase anisotropy to keep constant

But, bigger anisotropy—Need bigger fields to switch bit!
Engineering problem…

Thermal fluctuations: Problem in hard disk media, read heads

General concern in nanoscale devices!
Possible Solution: Spin Transfer

Electron spins become spin-polarized in direction of $M$: $M$ exerts torque

Reverse also happens: polarized spins exert torque on $M$
Spin-Transfer-Driven Switching

Sign of torque depends on direction of current: Causes magnetization motion

Bistable device: Current through device drives switching
High Speed ST-Switching

Pulse Amplitude
Current (mA)

-7.8
-6.2
-4.9
-3.9
-3.1
-2.5
-2.2
-2.0
-1.8

Switching Probability

0.0
0.5
1.0

Pulse Duration (ps)

100
1000
10000

7.8
6.2
4.9
3.9
3.1
2.5
2.2
2.0
1.8

Pulse Amplitude
Current (mA)

Quasi-static switching current

<300 ps switching time!

μ₀H = 66.7 mT

Katine HGST

30 nm

Pufall, THIC'05: 22
Spin Transfer Advantages

• Removes X-point field lines—simpler lithography, two terminal devices

• Becomes more efficient as devices shrink: Scalable

Fields: $\sim 1/d$

Spin Transfer: $\sim 1/d^2$
Spin-Transfer-Driven Oscillators

Monostable device (high fields): Current-tunable, Coherent, microwave magnetization precession

Electron current

applied field $H$

$\mu_0 H = 0.9 \ T$

$\begin{array}{c}
\begin{array}{c}
\text{Frequency (GHz)}
\end{array}
\end{array}$

$\begin{array}{c}
\begin{array}{c}
\text{Power (pW)}
\end{array}
\end{array}$

$\begin{array}{c}
\begin{array}{c}
\text{Current (mA)}
\end{array}
\end{array}$
Summary

MRAM is possible “universal” memory solution
  • “Spintronic” device: Uses e\textsuperscript{-} charge and spin
  • Fast (3-10 ns switching times)
  • Nonvolatile (magnetic storage)
  • Low power (no refresh)
  • Rad-hard (though supporting electronics aren’t!)

Toggle MRAM solves $\frac{1}{2}$-select problem

**Problem:** Must scale competitively with Si technology
  • Nanomagnetic elements sensitive to temperature
  • Complicated lithography

**Emerging technology solution:** Switching with Spin-polarized electron currents
### Memory Technology Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>NAND Flash</th>
<th>NOR Flash</th>
<th>1T1MTJ MRAM</th>
<th>XPC MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell Size in F²</strong></td>
<td>100</td>
<td>8</td>
<td>5</td>
<td>6</td>
<td>&gt;8 [published: 20-40]</td>
<td>&gt;4</td>
</tr>
<tr>
<td><strong>Supply Voltage</strong></td>
<td>2.5 V</td>
<td>2.5 V</td>
<td>1.8 V</td>
<td>3.3 V</td>
<td>1.8 V [published: 2.5-3.3V]</td>
<td>1.8 V</td>
</tr>
<tr>
<td><strong>Retention Power</strong></td>
<td>1.2W-375 mW</td>
<td>10 mW</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>Retention Time</strong></td>
<td>64 ms</td>
<td>10 yrs</td>
<td>10 yrs</td>
<td>10 yrs</td>
<td>10 yrs</td>
<td>10 yrs</td>
</tr>
<tr>
<td><strong>Random Read Access</strong></td>
<td>2-100 ns</td>
<td>60 ns</td>
<td>10 μs</td>
<td>90 ns</td>
<td>10ns-50ns [published: 3ns-50ns]</td>
<td>50 ns-1μs</td>
</tr>
<tr>
<td><strong>Random Write Access</strong></td>
<td>2-100 ns</td>
<td>60 ns</td>
<td>100 μs [erase 100 ms]</td>
<td>100 μs [erase 100 ms]</td>
<td>10-40 ns [published: 3ns-50ns]</td>
<td>20-40 ns</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>&gt;10¹⁵</td>
<td>&gt;10¹⁵</td>
<td>&gt;10¹⁵ read 10⁵ write</td>
<td>&gt;10¹⁵ read 10⁵ write</td>
<td>10¹⁵ [expected]</td>
<td>10¹⁵ [expected]</td>
</tr>
</tbody>
</table>

14. Comparison of memory technology.
A Brief History of MRAM

BIWB  Core memory, first disk drive, flat film, bubble, plated wire

1984-86 A. V. Pohm and Honeywell investigating radiation hard memory based on anisotropic magnetoresistance (AMR)


1989 NVE formed to develop AMR based MRAM

1990 IBM Spin Valve (B. Dieny, V Speriosou, S. S. Parkin, B Gurney et al.)

1994 IBM Spin valve MRAM patent (D. D. Tang et al. IBM)

1995 Magnetic Tunnel Junctions (MTJ) (Modera et al PRL 74, 3273, 1995)

1996 DARPA MRAM program: Honeywell (PSV), Motorola (PSV⇒MTJ) IBM (MTJ)

1999 IBM, Motorola MRAM working demos??

2002 Motorola goes to cladded write lines & tToggle write

2004 Motorola samples 4M MRAM chip

2004/2005 230% TMR in MgO MTJs; Spin transfer switched MRAM