Outline

- Corporate Overview
- Tornado 10™ Overview
- Applications
- Memory Configurations
- Data Storage Formats
- Typical Operation
- System Specifications
- Tornado 10™ Development Contract
- Tornado 10™ Advanced Development Model
- Tornado 10™ Production
- Pod Body Configuration
- Conclusion
Corporate Overview

• Founded in 1986
• Headquarters in Austin, Texas
• Professional Staff of Scientists & Engineers
• Capabilities
  - Systems Engineering
  - Electrical/Mechanical Design
  - ASIC Design
  - Prototype & Test Labs
  - Software Development
Objective

Develop a programmable, ultra high density recorder to capture and digitally store high speed video and instrumentation data.

Features

- Storage capacity exceeding 150 Gbits
- Input data rates up to 16 GBits/sec
- High speed parallel interface
- Industry standard interfaces (SCSI, DCRS, RS-422, etc.)
- Electrically compliant internal PCI slots
- CCSDS data formatting
- Data error encoding
- Non-volatile storage
- Lossless compression
Applications

Capture Ultra High Speed Data Sources
- Video (1024 x 1024 pixel x 1000 fps)
- Multiple independent data sources
  - 1 - 32 channels of 1 - 10 bit data at 50 MHz
- Wide Band Radar, Seeker Data

Capture PCI Compatible Data Sources
- SCSI, Fibre Channel, Ethernet, DCRsi™, 1553B
- Custom instrumentation interfaces

Flight Applications
- Size constrained applications ("Small Box" and pod mount)
- Environment-constrained applications (e.g., high ‘g’)

SPEC
Systems & Processes Engineering Corporation
Three Memory Configurations

**High Speed Memory**
- SDRAM Modules @ 3GBytes Per Module (64Mb SDRAM)
- High Performance, High Capacity

**High Speed Memory with Nonvolatile Backup**
- SDRAM & EEPROM Modules
- High Performance, Less Capacity
- SDRAM contents transferred to EEPROM after capture

**Low Speed Nonvolatile Memory**
- EEPROM Modules
- Low Performance, High Capacity
Data Storage Formats

Data stored in user selectable compressed or uncompressed format

Compressed data packets stored in non-sequential order (packets written to memory when complete)
- Maximum storage capacity
- Fast sequential access
- Slower random access (packet search required)

Uncompressed data packets stored in sequential order
- Less storage capacity
- Fast sequential access
- Fast random access
Typical Operation

Capture 10 - 20 s of High Speed Data (e.g. Video)
  • Lossless compression 2:1 on average, ~7:1 maximum
  • Packetize compressed data
  • Store in SDRAM

Data Retrieval
  • Controller reads data over 256-Bit Memory Bus
  • Controller uncompresses/error corrects/formats data
  • Controller transfers formatted data over PCI bus
    - SCSI to tape backup or PC
    - DCRsi™ to tape backup
    - Ethernet to workstation
# Tornado 10™ System Specifications

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Chassis</td>
<td>ATR Short (Long Option)</td>
</tr>
<tr>
<td>Weight (without memory)</td>
<td>18 lbs</td>
</tr>
<tr>
<td>Max Memory Modules</td>
<td></td>
</tr>
<tr>
<td>- 1 ATR Short</td>
<td>5 modules (15 GB)</td>
</tr>
<tr>
<td>- 1 ATR Long</td>
<td>9 modules (27 GB)</td>
</tr>
<tr>
<td>Memory Module</td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td>5 lbs</td>
</tr>
<tr>
<td>Capacity</td>
<td>3 GB (with 64 Mbit TSOPs)</td>
</tr>
<tr>
<td>Memory Type</td>
<td>SDRAM or EEPROM</td>
</tr>
<tr>
<td>Cooling</td>
<td>Conduction</td>
</tr>
<tr>
<td>Environment</td>
<td>Flight</td>
</tr>
<tr>
<td>Data Rate</td>
<td></td>
</tr>
<tr>
<td>High Speed (sustained)</td>
<td>10.4 Gbps</td>
</tr>
<tr>
<td>High Speed (burst)</td>
<td>16 Gbps (32 ch x 10-bit x 50 MHz)</td>
</tr>
<tr>
<td>Low Speed Data/Control</td>
<td>1 Gbps (PCI 32 bit x 33 MHz)</td>
</tr>
</tbody>
</table>
Developed system architecture for pod body implementation
  • Based on chip scale packaging techniques
  • ASIC implementation of special functions

Developed detailed design of pod body architecture in lower risk “small box” format
  • FPGAs used instead of ASICS
  • Memory in TSOPs vs. chip scale package
  • Fulfills a number of recording needs

Performed development risk reduction effort
  • Utilized simulation tools to verify design
  • Particularly challenging parts of the design were implemented in the Advanced Development Model (ADM)
Tornado 10™ Advance Development Model
ADM Memory Card

Front Side

- Memory Controller
- FPGA (Super BGA)
- Clock
- Serial EPROM
- Elastomeric Interconnects
- Bus Terminators
- SDRAM (32 TSOPS per side)
- Transceivers (16 per side)

Back Side

SPEC
Systems & Processes Engineering Corporation
Risks Mitigated by ADM

- Implementation of design in FPGAs
  - Memory controller functionality verified
  - Memory controller will operate at required speed
- Extreme Bus™ memory data bus has been proven
- Captured data in memory and extracted
- Resolved memory card and controller interface issues
- DCRsi interface developed
- Proven system clock circuit
- Thermal management techniques proven
- ECPI scheme has been proven
Tornado 10™ Production

DOD - TTD&D (Test Technology Development & Demonstration Contract)

- Production model
- High speed front end implemented in ASICs
- Memory Module Upgraded from 512 Mbytes to 3 Gbytes
- Faster FPGAs for Memory Module to meet 16 Gb/sec requirement.
- Detail Pod Body Design Study
SPEC Integrated Instrumentation System

- DATM Card Set
- DATM Chip Set
- Commercial Markets
- Missile Pod Instrumentation
- Aircraft/Ground Instrumentation
- Missile Pod Body Recorder
- Production SSDR
- Size Reduction
- Size Reduction
- Integrated System Development
  - DATM Card Set Development
  - TTD&D Program
- Enhancement
- Enhancement
• The SPEC Tornado 10™ meets the need for High Speed, High Density Recording Applications

• “Small Box” Production Model Available 4Q /98

• Miniaturization Path to Pod Body recorder

• SPEC is exploring partnership/licensing options