LINEAR DIGITAL RECORDER WITH 100 MBYTE/SEC HIPPI INTERFACE

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SUMMARY

A plan has been formulated and selected for a NASA Phase II SBIR award for using the VLBA tape recorder for recording general data. The VLBA tape recorder is a high-speed, high-density linear tape recorder developed for Very Long Baseline Interferometry (VLBI) which is presently capable of recording at rates up to 2 Gbit/sec and holding up to 1 Terabyte of data on one tape, using a special interface and not employing error correction. A general-purpose interface and error correction is being added so that the recorder can be used in other high-speed, high-capacity applications.

RECORDER CHARACTERISTICS

The VLBA recorder was developed specifically for recording VLBI data using the Very Long Baseline Array of radio astronomy antennas built by the National Radio Astronomy Observatory. It is an evolution of the technology developed for the NASA Mark IIIA VLBI recording system at MIT Haystack Observatory. Its characteristics may be summarized as follows:

Recording medium:	1-inch-wide D1-equivalent 16 μm thick tape
Head type:	38 μm width, single-crystal ferrite
Bit density:	56,000 flux transitions per inch
Format:	continuous linear tracks, NRZM, magnetic saturation
Tape speed:	For 9 Mbit/sec data, 160 inches per second
MTBF:	10,000 hours typical
Head life:	5,000-20,000 hours depending on environment
Head replacement cost:	~$1/hour per 34-track headstack
Maintenance:	headstack and tape path cleaned with a cotton swab at each tape change.

A single headstack writes and reads 34 data tracks at a time. The heads are 38 μm wide and are separated by 698.5 μm, so that potentially 698.5/38 = 18.38 passes could be written on the tape. However, some allowance for guard bands between tracks must be made, since the magnetic gap is exactly perpendicular to the direction of tape motion and there must be no crosstalk between tracks. A practical limit is 16 passes, which gives a track spacing of 43.7 μm with a guard band of about 5 μm. There are thus 544 data tracks on the tape. Future improvements in tapes and heads are expected to increase this number.

The tape is a D1- or S-VHS equivalent tape available from both 3M and Sony. This tape is 16 μm thick, and 20,500 usable feet are contained on a 16-inch reel (only 14-inch reels are currently used). The bit density supportable on this tape is 60,000 bits per inch, so each track contains 14.4 Gigabits. The whole tape with 544 tracks then holds about 8.03 Terabits, or one Terabyte. Using the error-correcting format being developed, this becomes 788 Gbytes of user data. The cost of one reel of this tape is presently about $1500, or $1.90 per Gigabyte. At the maximum user data rate supported by one headstack, namely 69.44 Mbyte/sec, one tape lasts approximately 192 minutes. Up to 4 headstacks may be mounted on one transport, yielding an aggregate recording rate of 278 Mbyte/sec with a recording time of 48 minutes. This is also the time required to duplicate a tape.

Typical tape life is several hundred read-write cycles including shipping once per month in uncontrolled conditions.

INTERFACES

The data interface in the present VLBA recorder is a set of parallel data lines, each supplying data directly to a single head in the headstack. Formatting of the user data consists of adding synchronization words, time codes, identification data, and parity bits in an external formatter. These bits are simply transferred directly to tape. On playback, the signals from each head are amplified, equalized, and routed to bit synchronizers which recover the clocks from each data stream. All further processing is performed in an external unit which recovers the synchronization codes, de-skews the tracks, and combines the data into a desired format.

In the system under development, the recorder will be responsible for all functions of formatting and deformatting. The user will supply data over a standard interface and recover data from the recorder over the same interface.

For the data rates of concern, there is a prime “standard” interface, namely the High-Performance Parallel Interface, or HIPPI, defined in ANSI X3.183-1991, as defined by the ANSI Task Group X3T9.3. We have adopted this interface as the standard recorder data interface for both record and playback for all applications. The HIPPI channel consists of 32 balanced ECL signals with a common 25 MHz clock and a transfer protocol allowing bursty transmissions. For applications requiring less than the full channel capacity, fewer tracks than the maximum will be written, giving 800, 400, 200, and 100 Mbit/sec HIPPI transfer rates.

The HIPPI channel is a one-way device, so two HIPPI channels are needed in order to accommodate both record and playback functions. Commercially available chips provide a single 100 Mbyte/sec HIPPI interface. In the prototype system, two headstacks will be employed, enabling a maximum of 138.88 Mbyte/sec to be recorded. Since the recorder speed can be set with very fine resolution, it will be chosen such that the bit density remains at 56,000 bits per inch.

Since other high-speed protocols and fiber optic interfaces such as advanced ATM are coming into use, it is essential that the recorder be expandable to accommodate them. The plan is eventually to add, for example, an ATM-to-HIPPI interface and continue to operate the recorder exclusively from the HIPPI interface. This simplifies the interfacing problem by placing it outside the recorder proper.

A single low-speed interface will suffice to set the recording mode and control the playback process. This will be a 9600 baud RS-232C interface, permitting operation by any computer.

ERROR CORRECTION

For an individual tape track, which is the minimal recording sub-channel, the important characteristics for the VLBA recorder as it is presently used are as follows:

Random errors:	Bit Error Rate (BER) $<3 \times 10^{-4}$ with 10-year-old tape; typically 3×10^{-6} with new tape, 3×10^{-5} with 3-year-old tape
Burst errors:	Typical length 100-1000 bits; typical rate 1 burst in 10^7 bits; bursts usually cause loss of bit synchronization

Random errors are caused by low signal-to-noise ratio (SNR), imperfect equalization, and imperfect bit synchronization. Burst errors are caused primarily by tape defects and are consequently highly dependent on the particular tape in use; any system of error correction must accommodate the worst-case tape. In order to minimize the data lost to dropouts, the distance between sync words should be comparable to the size of the dropouts.

For typical imaging data, a bit error rate better than 1×10^{-9} is required. Other applications require bit error rates as low as 1×10^{-13}.

Recently, VLSI chip sets which implement Reed-Solomon error correction algorithms have become available, and some can run at the data rates in which we are interested. Such chips are available from such manufacturers as LSI Logic and CNR, Inc. It appears that suitable devices for this application are available from Advanced Hardware Architectures (AHA). We will use the AHA4011 device, which has the following characteristics:

Input data format:	8-bit parallel (byte organization)
Data rate:	10 Mbyte/sec (80 Mbit/sec)
Max block length:	255 bytes (programmable)
Max errors correctable:	10 per block (or 20 erasures)
Other features:	No external buffers or control required
Cost:	$20 each in large quantities

Data will first be coded into data blocks of length 235 bytes. For each such block, we will program the AHA4011 to add 20 error correction bytes to make the total block length 255. This is an overhead of 8.5%.

This scheme will permit correction of up to 10 errors or 20 erasures (or a linear combination of both). Even with a raw bit error rate of 1×10^{-4}, the corrected code block error rate is predicted to be 7×10^{-15}, which satisfies our requirements. The errors will be decorrelated by interleaving the data over a distance long enough so that only one or two bytes from each code block are contained within a single error burst.

CONFIGURATION

The VLBA recorder uses a Metrum Model 96 tape transport, which is a full-size rack of hardware. In the new configuration, it will contain:

VME-based control computer
HIPPI interfaces with buffers
Error correction/formatting boards
Analog write drivers
Analog playback amplifiers/equalizers
Clock recovery (bit sync) boards
Deskewing buffers
Transport and headstack motion controllers
Power supplies

The prototype system will be equipped with two headstacks and so will be capable of recording up to about 144 Mbyte/sec of user data. Adding two additional headstacks and supporting electronics could bring the total to 288 Mbyte/sec.

RECORDING AND PLAYBACK PROCESS

In addition to error correction, some formatting must be introduced in the form of synchronization words, modulation, and longitudinal parity. Sync words are absolute identifiers of tape block start points. Data modulation by a pseudo-random sequence will guarantee roughly equal numbers of ones and zeroes in the data regardless of content. The addition of longitudinal parity bits on each track will force sufficient transitions in the NRZM format so that good bit synchronizer performance can be maintained.

Upon playback, the parity, modulation, sync, and other formatting information must be undone and stripped out, and the error correction bytes used to restore the original user data. This data must then be reformatted so that it can be transmitted over the HIPPI interface back to the user. A summary of the recording and playback process is shown as Figure 1.

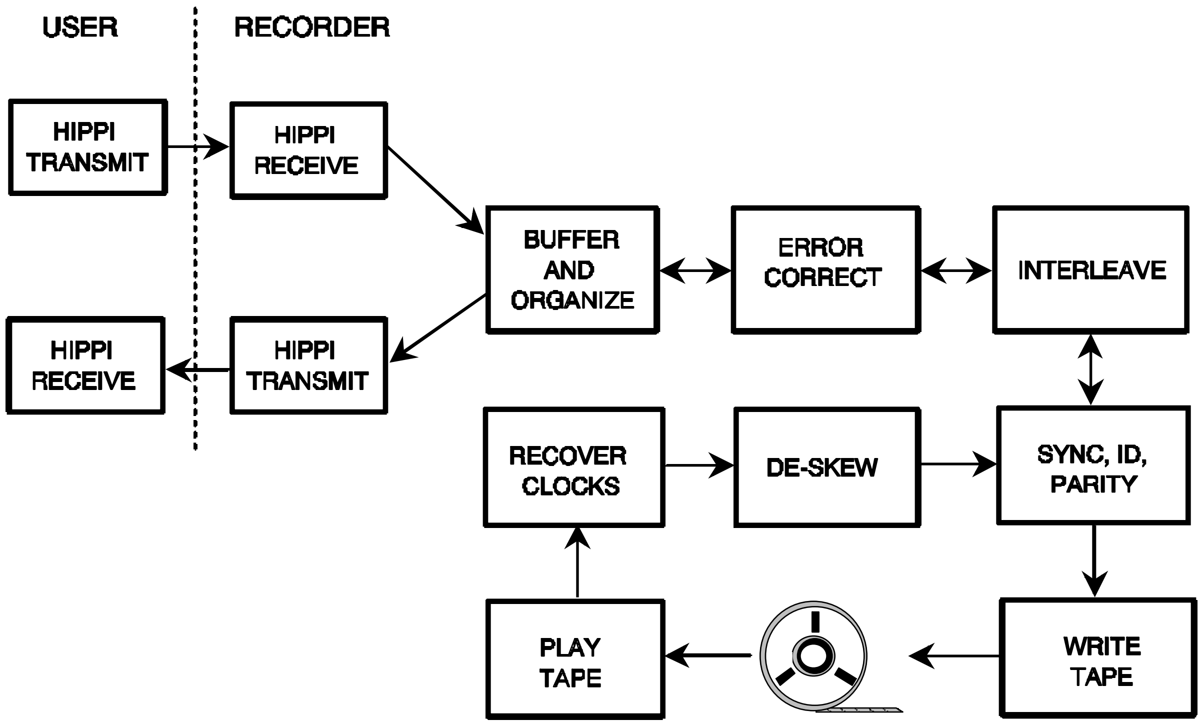

Figure 1. Data flow to and from the recorder

In much of the recording and playback electronics, the same circuitry can be used to perform both the recording and playback processing.

DEVELOPMENT STATUS AND SCHEDULE

The standard parts of the recorder are about 90% complete and mostly tested as of this date (2 April 1996). The top level designs of all the new electronics are complete. The HIPPI interface design is complete and ready for fabrication; it should begin testing this month, using an Essential Communications HAPPI HIPPI tester as the source and destination for HIPPI transmissions. The detailed design for the error correction and interleaving board is nearly complete. Detailed design on the formatting and deformatting system should begin in May 1996. Some of the control software definitions are in place and some control software has been written. The completion target date for the prototype recorder is September, 1996.

FUTURE USES

We anticipate that a recorder capable of 288 Mbyte/sec record rate will find many uses. Large data bases such as scientific data, medical images, and satellite data come to mind immediately. Special high data rate applications in science and engineering are also potential users, including radio astronomy, particle accelerators, and wind tunnels. It is conceivable that high data rate networks would also find the recorder of use, although it will probably be necessary to add a large memory buffer to the system in order to use what is essentially a streaming tape drive in an application with intermittent recording requirements.

PLANNED FUTURE IMPROVEMENTS

There are a number of possible improvements in development or under consideration. A thin-film head array would make possible track width reduction from the present 38 μm to 4 μm using present tape, achieving the same SNR as at present. It would also make possible the use of higher coercivity, higher SNR, finer grain tapes such as barium ferrite and metal particle (W-VHS or equivalent). Improvements in tracking would allow reduction of track width to 1 μm; coupled with the advanced tape, this would make possible a volume density of 1 bit per μm^3, resulting in up to 100 Tbytes on one tape volume within a few years.

Also under consideration is a mechanical redesign of the tape transport, which would retain the excellent tracking characteristics of the present Metrum transport in a new, compact package. This would allow use of the high density tape format in some applications requiring transportability, and the option of using tape cartridges with a robotic changer and automatic loading.

REFERENCES

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